Automotive high-voltage electronic fuse demonstrator

User guide

About this document

Scope and purpose

This eFuse proof of concept implementation demonstrates the features of a high-voltage (HV) solid state fuse for DC currents, e.g., auxiliary loads in an electric or hybrid vehicle. It incorporates a variety of diagnostic features, e.g., short circuit protection for safe and fast turn-off and in-situ device diagnostics. This user guide shall give a brief overview about the concept and functions implemented, as well as instructions for operating the system.

The eFuse proof of concept system consists of:

- Output stage (different technologies and output power configurations possible)
- Driver/Mainboard (discrete driver implementation and functions)
- Interface board (galvanically isolated interface to the PC)

Intended audience

Users of the demonstrator boards and hardware developers.

Reference board/kit

Product(s) embedded on a PCB, with a focus on specific applications and defined use cases that can include Software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI, and quality standards (for example UL, CE) requirements.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *Only personnel familiar with the load, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A load that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the load, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Application overview

1.1 Introduction to eFuse

The supply and the wiring harness of a high-power source must be protected against overload conditions and short circuits, as errors such as these of each individual branch could cause a fatal malfunction of the complete system. In order to keep the remaining system functional, each branch should be protected with an individual safety element.

The legacy overload protection device for a wiring harness and protecting the system is a melting fuse (or a pyro-fuse if fast turn off time is required). In the case of an overload or short circuit event the fuse will melt and disconnect the malfunctioning device from the system. In this case, the fault device is disconnected and is no longer functional.

A melting-fuse or pyro-fuse is a one-shot device, which means that when it has been triggered, the fuse must be replaced manually. Furthermore, the trigger characteristic of a conventional melting fuse is slow and the actual switch off current is orders of magnitude higher than the nominal current. In this case it must be ensured that such high trigger current can be handled and supplied by the system and the wiring harness. The tripping characteristic and short circuit currents of a semiconductor-based fuse compared to a melting fuse are shown in **Figure 1**. In this example, due to the slow reaction time of a melting fuse the maximum short circuit current is ~2 orders of magnitude higher than with an eFuse.

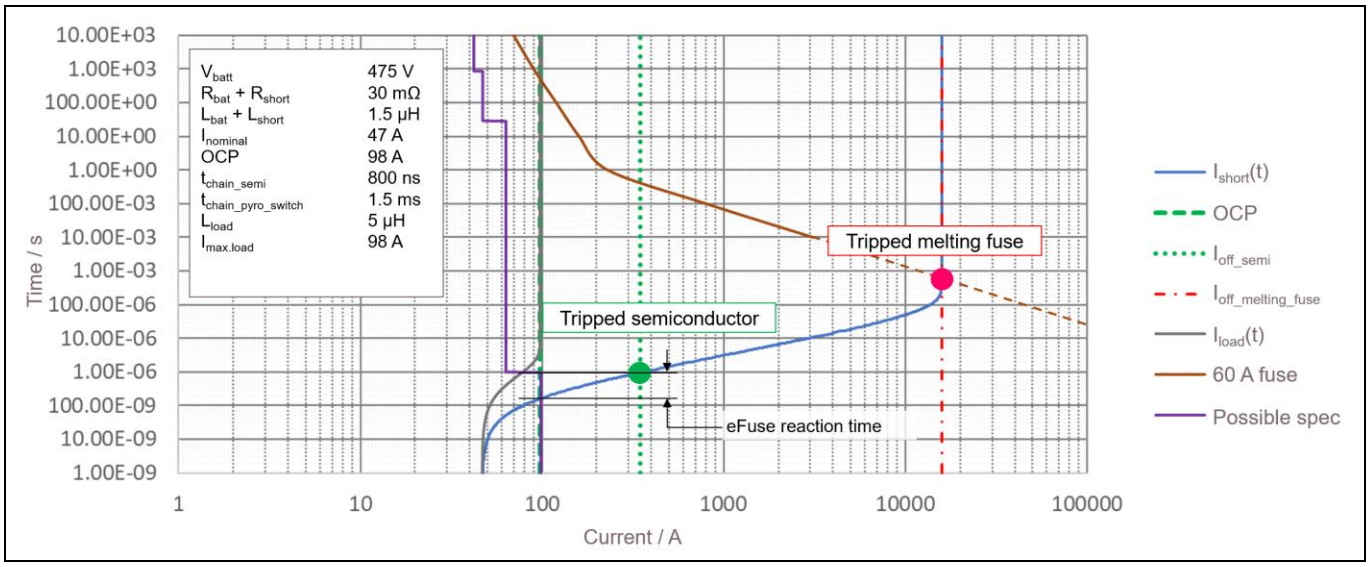

Figure 1 Tripping characteristics comparison of an eFuse vs. a melting fuse

The melting fuse is a passive element without any diagnostic functionality. This means that any diagnostic or intelligent functions (e.g., detecting that the fuse has been triggered) must be built externally.

As the trigger of a melting fuse is dependent on the energy required to melt the fusing element, the trigger current is affected by the ambient temperature. The ambient temperature effect is in the range of +/- 10 ... 20 percent of the nominal rated trigger current. Another drawback of a conventional melting fuse is the possible mechanical fatigue when the fuse is loaded with pulsed currents. These electrical pulses caused, e.g., by surge currents, start-up currents, inrush currents or transients produce a thermal cycling in the fusing element, which can cause a degradation of the metallic fuse element, in turn reducing the current carrying capabilities. **[1]**

To manually replace the melting fuse, it must be accessible from the outside and maintenance openings must be incorporated into the design. Therefore, replacing the melting fuse by an electronic fuse (eFuse) offers numerous benefits:

- The eFuse is maintenance free with no mechanical replacement needed
- Configurable overload detection and pre-warning
- Diagnostic functions easily implementable
- If triggered, reset possible via software commands
- No performance degradation because of current induced stress
- Selective arc-free switch-off in case of failure

The main difference between an eFuse and a load switch or solid-state relay is that the eFuse is used as a safe disconnecting device and is not designed to switch on capacitive loads. This means that high inrush currents (e.g., due to capacitor charging currents) could cause a tripping of the eFuse, and therefore the turn-on of the fuse should be done with no- or low-load currents.

1.2 Automotive eFuse application example

In electric or hybrid vehicles, an increasing trend toward electrification of auxiliary loads to the HV supply rail can be observed. Malfunction of these auxiliary loads could compromise the availability of the HV boardnet and functions driven from this supply rail. In order to minimize failure propagation into the vehicle network, the auxiliary loads are protected with an eFuse. In this case the malfunctioning branch can be disabled individually and all other functions will remain fully operational. As those functions could include safety-relevant systems (e.g., main drive), the disconnect function of the failed branch is a safety-relevant function as well, with a dedicated ASIL rating.

For high-availability functions, e.g., DC-DC converter for replacing the 12 V battery in an electric vehicle, a redundant approach is typically used. In this case it is key to be able to switch to the backup converter very quickly if there is a malfunction in the primary converter. Such fast transitions and additional features, e.g., deactivation of the second converter in normal operation, can only be achieved with a solid-state solution.

The automotive boardnet usually consists of the HV battery and one or two battery main switches as shown in **Figure 2**. The battery main switch is used to power up the HV net and the main drive of the vehicle. The remaining auxiliary loads are protected by either a centralized or decentralized eFuse.

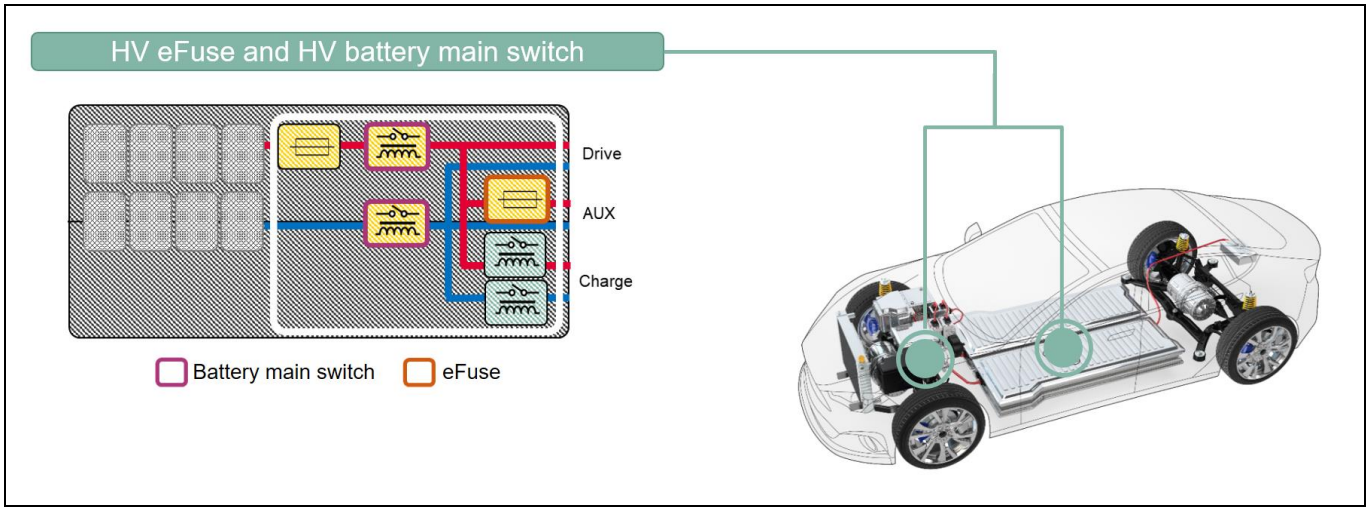

Figure 2 Automotive board net with battery main switch and eFuse application

Figure 3 shows centralized and decentralized eFuse implementation options. A centralized eFuse is placed within the power distribution unit and has higher current capabilities than a decentralized eFuse. In a decentralized eFuse topology, the eFuse could also be part of the auxiliary control unit itself (e.g., DC-DC converter, HVAC compressor, etc.). In both cases the eFuse could re-use the existing infrastructure of the electronic control unit (ECU) e.g., battery main switch, power distribution unit, or on-board charger.

Depending on the individual application requirements, an eFuse could be implemented as a uni-directional or bi-directional switch. For a bi-directional application, the MOSFETs in the output stage will be placed in a back-to-back configuration (series connection of two MOSFETs, connected at the source).

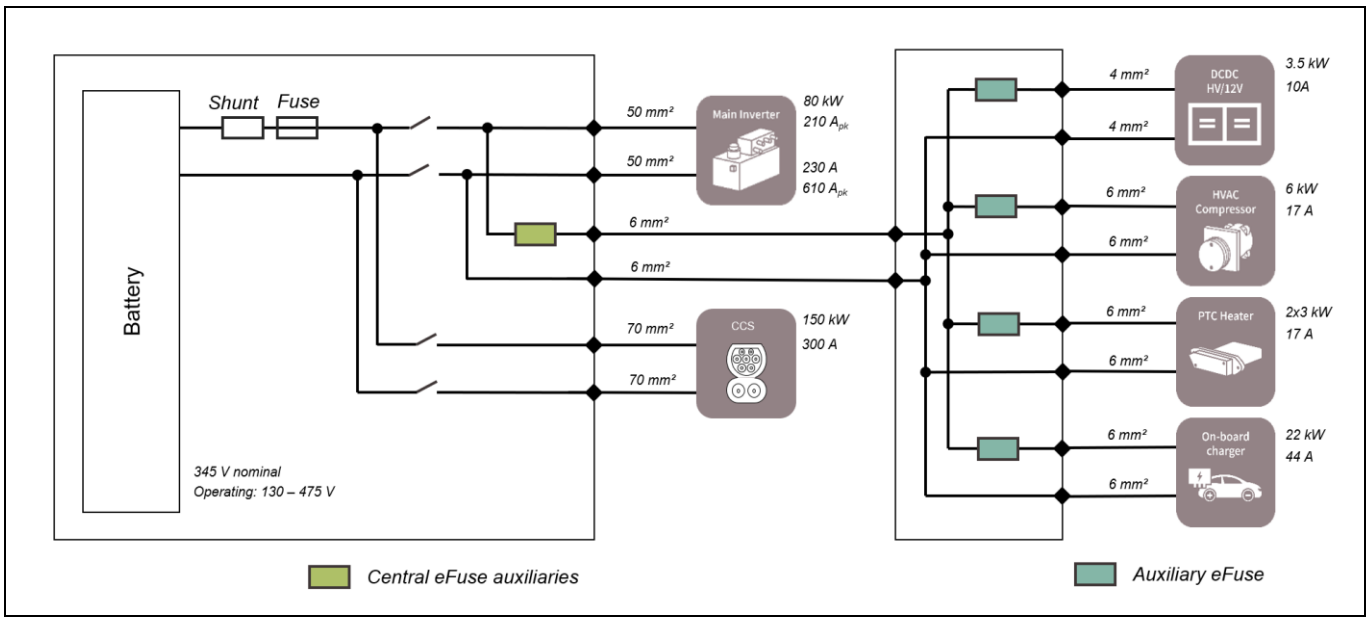

Figure 3 Centralized and de-centralized eFuse implementations

1.3 Typical boardnet topology for a centralized eFuse

In a typical automotive boardnet configuration, the battery is disconnected from the main system with one battery main switch on the high-side (e.g., eDisconnect switch with additional pre-charge circuit) and one switch on the low-side (e.g., mechanical relay). The main inverter is then directly connected to the main grid after the battery main switch.

Auxiliary fuses are typically implemented into one supply line (either high side or low side). In the case of a centralized auxiliary fuse, the connection point to the main powertrain can be close to the battery main switch and is thus close to the connection point of the main inverter. **Figure 4** shows a typical boardnet topology with the eFuse connected on the low side terminal of the auxiliary load. The loads are connected with HV power cables, which imply parasitic impedances depending on the wire diameter and length. Both branches and their respective impedances must be considered for the equivalent circuit diagram of the HV boardnet.

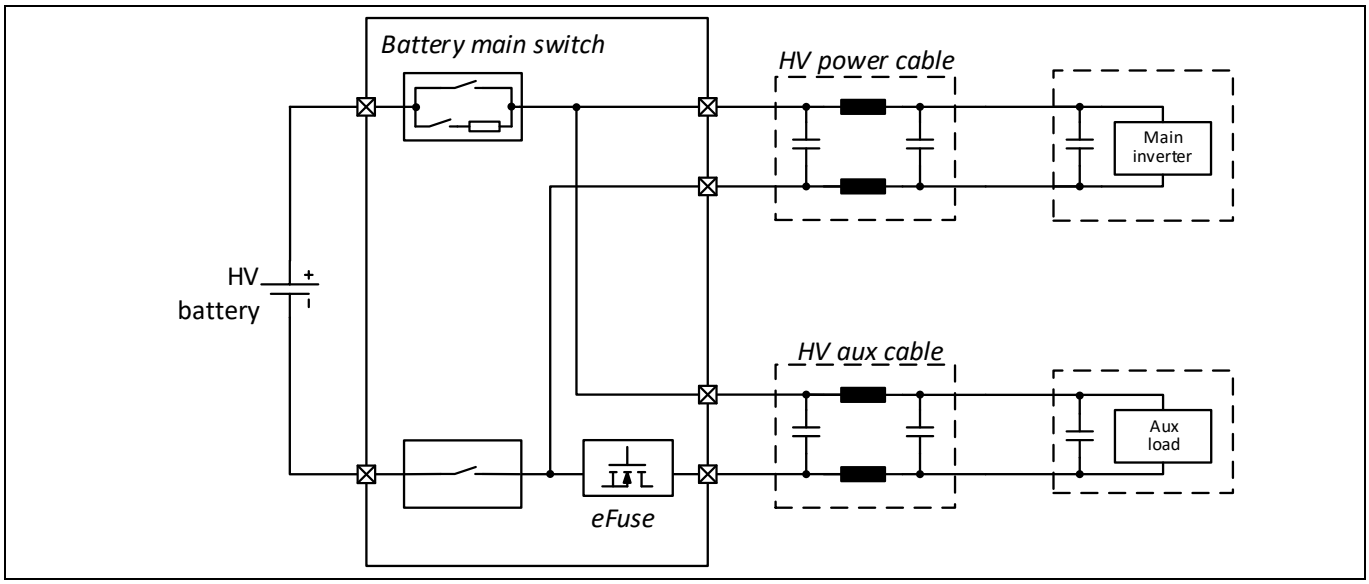

Figure 4 Typical boardnet topology with eFuse in low-side configuration

1.4 Example eFuse load profile

In a centralized eFuse implementation as shown in **Figure 5**, all auxiliary loads are connected on a single branch from the HV battery. **Table 2** shows the nominal power rating and the load current for a dedicated load at the nominal battery voltage. For limited time the peak current of those loads could be higher – e.g., the peak power of a DC-DC converter could be increased to 4 kW for 10 seconds. This results in a typical load profile for a centralized eFuse implementation as shown in **Figure 6**.

In this case it could be differentiated between different load conditions as shown in **Table 3**. With this load pattern, a 42 A DC rated eFuse must be able to handle significant overload currents up to 68 A_{RMS} for 10 s. Additionally, the typical load pattern includes a significant AC superimposition for all load ranges (see **Chapter 1.5**). In this example, the worst-case AC amplitude of the ripple current is defined with 26 A_{pk}. This not only affects the thermal design, but also the protection mechanisms as those ripple currents will not trigger the fast overcurrent detection (OCD) of the eFuse, the OCD threshold needs to be set to more than 89 A. When considering all tolerances of the current measurement and threshold level setting, the nominal overcurrent detection level needs to be at least 110 A in order to not trigger in normal operating conditions.

As the thermal design of the eFuse is dimensioned for 42 A continuous current (including limited-time overload patterns) but the overcurrent threshold needs to be set to at least 110 A, an additional protection mechanism to cover the current range between those limits is needed. In this case the power devices are thermally limited

and should be protected to not reach the limit load integral (i^2t value) of the output stage and in that case a destructive chip temperature. This could be done by integrating the current and calculating the temperature rise with respect to the $R_{DS(on)}$ and thermal mass m and thermal capacity c, accordingly:

$$E = \int_0^{t_1} R_{DS(on)}(T) \cdot i^2 dt \quad \rightarrow \quad \Delta T = \frac{E}{m \cdot c}$$

As these calculations include uncertainties and tolerances this method will lead to significant errors in the temperature calculation. These errors need to be considered in the thermal design and lead to an over dimensioning of the output stage and therefore higher cost. Direct thermal monitoring of the die temperature is the best method to protect the output stage during these operating conditions and resulting in an optimized utilization of the power device.

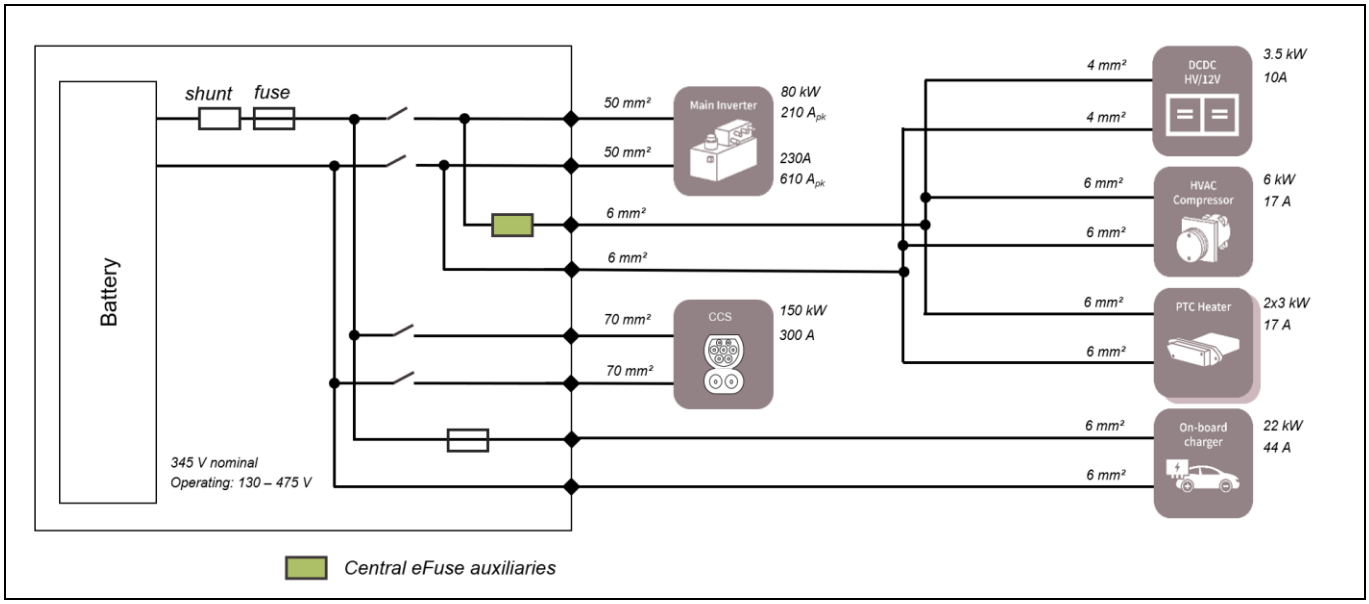

Figure 5 Connected loads for a centralized eFuse

Table 2 Loads connected for the central eFuse example

Auxiliary load	Nominal power rating	Nominal load current
PTC heater 1	3 kW	8.5 A ($V_{bat,nom}$ = 345 V)
PTC heater 2	3 kW	8.5 A ($V_{bat,nom}$ = 345 V)
HVAC compressor	6 kW	17 A ($V_{bat,nom}$ = 345 V)
HV/12 V DC-DC converter	3.5 kW	10 A ($V_{bat,nom}$ = 345 V)
Total Power for Centralized eFuse	***14.5 kW***	***44 A***

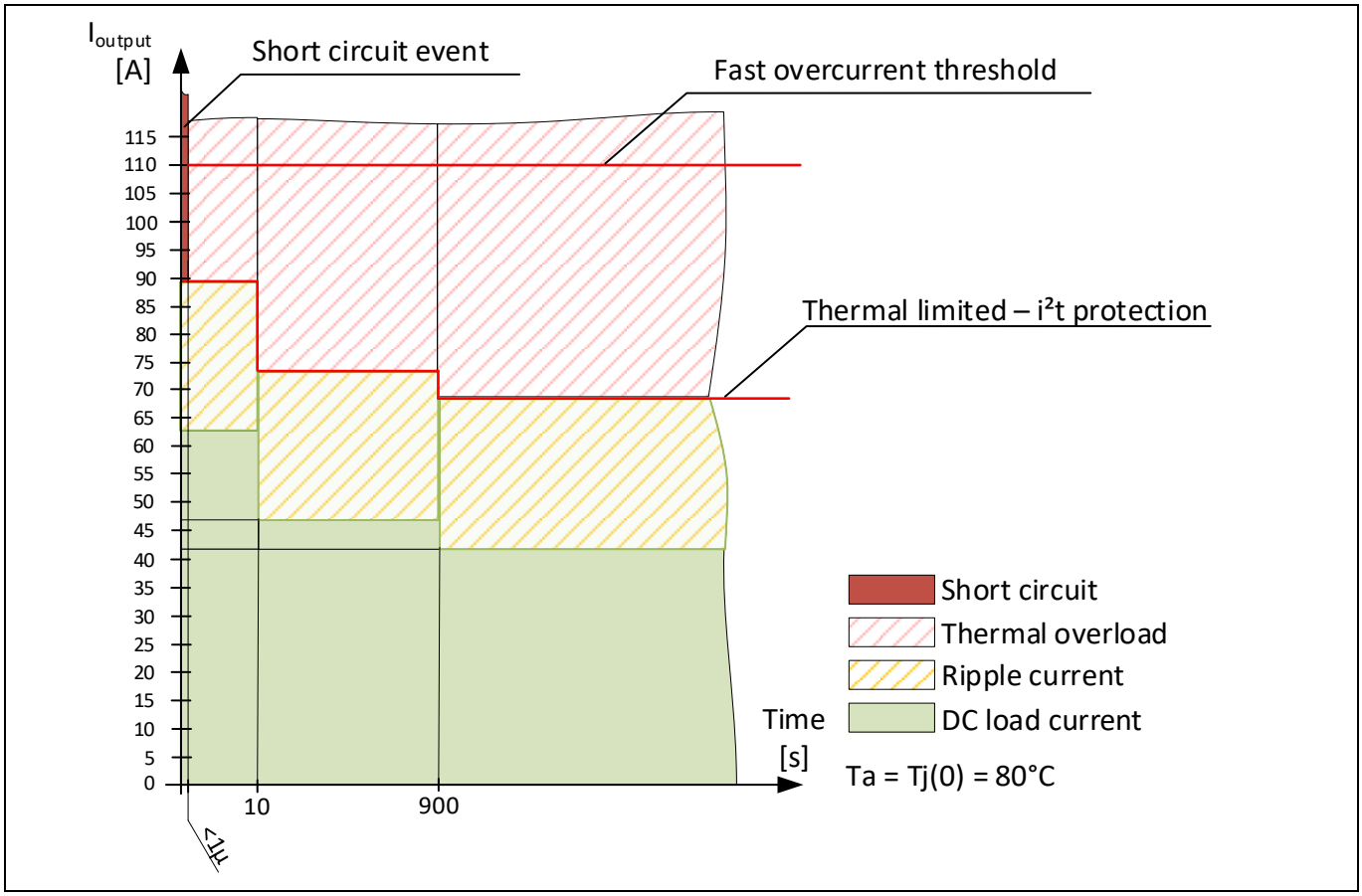

Figure 6 Load profile for centralized eFuse

Table 3 Centralized eFuse load pattern

Duration	Nominal Load	Load including ripple current
Infinite	42 A	68 A
900 s	46 A	72 A
10 s	63 A	89 A
Less than 1 µs	More than 120 A	-

1.5 Load pattern in an application environment

An eFuse has a different, much faster trigger characteristic than a melting fuse as discussed in **Chapter 1.1**, the type of connected load must be taken into consideration in the design. When using a traditional melting fuse, the trigger threshold is defined by the energy level needed to trigger the fusing element. This intrinsic integration is no longer the case with an eFuse, and therefore the load current pattern needs to be considered.

In a typical eFuse application, the protected load could include auxiliary inverters (e.g., pump, motor) or switched power converters (e.g., onboard charger, DC-DC converter). This type of applications usually consists of a DC-link bulk capacitor and a switched output stage (e.g., B6 inverter stage, H-bridge). Such a topology for a B6 inverter stage is shown in **Figure 7**.

When the inverter is in normal operation, the voltage on the output phase V_{phase} is pulsed with the frequency of the PWM output of the controller. This PWM frequency is for drive applications usually from 6 kHz up to 20 kHz, with the tendency for this to increase when using wide-bandgap power devices (e.g., SiC, GaN).

Although the DC-link capacitor is low-pass filtering the input current from the HV battery, a significant ripple current is still drawn from the HV system. As this ripple current contributes to the RMS current of the eFuse, it must be taken into consideration when dimensioning the cooling strategy and tripping characteristics of an eFuse.

Furthermore, it is important that no protection and diagnostic mechanisms of the eFuse are triggered by these ripple currents from the load.

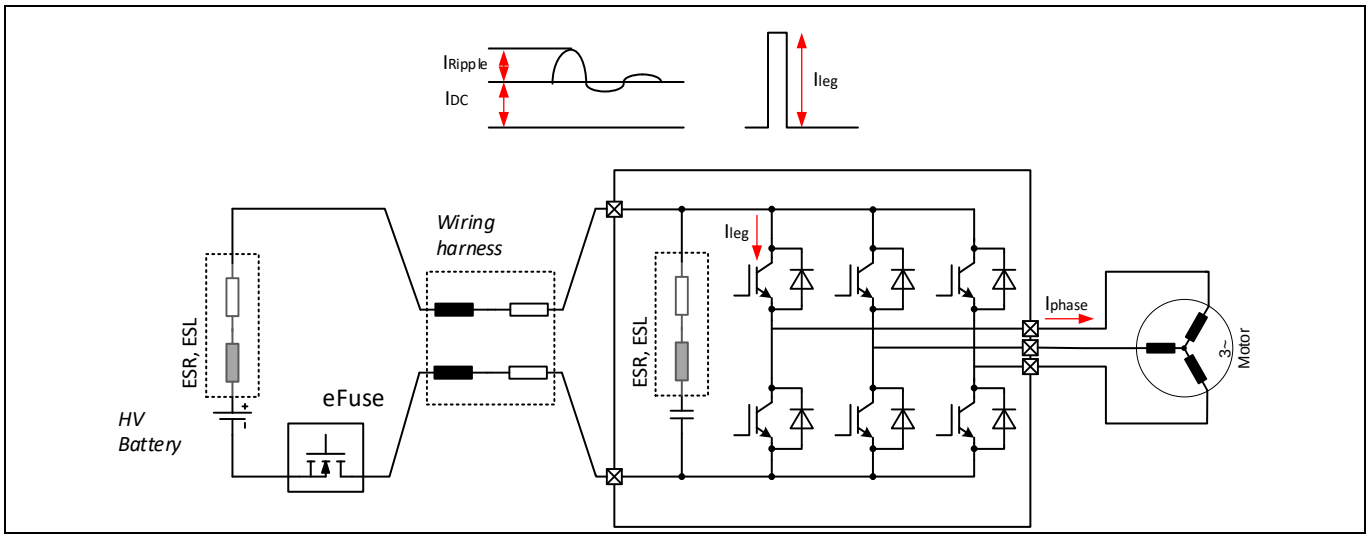

Figure 7 Typical topology for an eFuse application

As discussed, due to these pulsed current patterns, the load current may have a significant AC content. The frequency spectrum of this load current AC share depends on different parameters of the system:

- Output current shape of the inverter (e.g., rectangular, triangular)
- Switching frequency
- Input current filter
- DC-link capacitor (ESL, ESR)

The load current can be modelled as a DC current superimposed with an AC ripple as shown in **Figure 8**. For a drive inverter the input current of the output stage is a rectangular shape, while for a DC-DC converter the shape is usually triangular.

As the input low-pass filter with the DC link capacitor will already dampen the AC component of the load input current significantly, the maximum amplitude of those ripple currents is limited. The AC content of the load current of a drive inverter will therefore have a trapezoidal shape, resulting in a lower harmonic component in the amplitude spectrum. This generalized example considers a worst-case scenario with a rectangular AC ripple component.

The Fourier transform of an ideal rectangular waveform with the amplitude of 1 would be:

$$x(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{\sin\big((2k-1)\omega t\big)}{2k-1} = \frac{4}{\pi}\left(\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + \cdots\right)$$

For an ideal triangular waveform the Fourier series would have a 1/θ² roll-off:

$$x(t) = \frac{8}{\pi^2}\sum_{k=1}^{\infty}(-1)^k\frac{\sin\big((2k+1)\omega t\big)}{(2k+1)^2} = \frac{8}{\pi^2}\left(\sin(\omega t) - \frac{1}{9}\sin(3\omega t) + \frac{1}{25}\sin(5\omega t) - \cdots\right)$$

The spectral distribution of the current (amplitude spectrum) of a drive inverter is shown in **Figure 8**. **Table 4** shows the load characteristics with AC content for typical auxiliary loads.

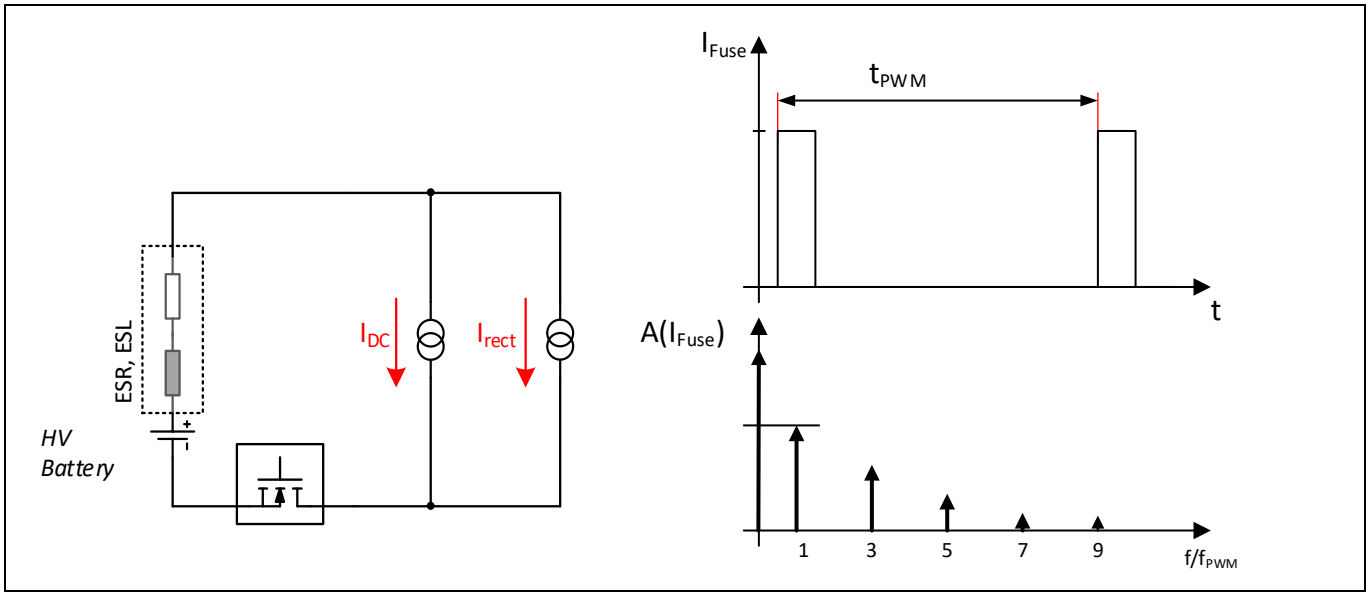

Figure 8 Load current equivalent circuit and load profile

Table 4 Parameters of typical auxiliary loads

Load type	f(PWM)	Spectrum roll-off	Amplitude factor at f(PWM)
Drive inverter	6 kHz…20 kHz	Rectangular waveform - 1/θ	4/ π
DC-DC converter	100 kHz…500 kHz	Triangular waveform - 1/θ²	8/ π^2
Heater	No AC content	-	-

With these considerations of the amplitude response for different auxiliary load currents, the maximum current slew rate during normal operation can be defined. Up to this slew rates the eFuse should not be disturbed, especially the OCD.

The maximum slew-rate to be considered for the OCD of a sine waveform can be calculated as followed:

$$i(t) = I_{pk}\sin(\omega t)$$

$$\frac{di}{dt} = \omega I_{pk}\cos(\omega t)$$

Maximum slew rate is at the zero crossing of the sine wave:

$$\left(\frac{di}{dt}\right)_{max} = \omega I_{pk}$$

The slew rates in an eFuse application with the maximum switching frequencies for the fundamental, third- and fifth- order harmonics are shown in **Table 5**. For this example, a typical auxiliary inverter with 6 kW power rating and a typical DC-DC converter with 4 kW power rating is used. The amplitude roll-off factors of the Fourier series as described above are used.

Table 5 Maximum switching frequencies

	Auxiliary inverter			DC-DC converter		
Harmonics	**f/Hz**	**$\|I_A\|$/A**	**di/dt/A/µs**	**f/Hz**	**$\|I_A\|$/A**	**di/dt/A/µs**
f_0	20.000	30.6	3.85	500,000	15	47
3	60.000	10.2	3.85	1,500,000	1.7	15.7
5	100.000	6.1	3.85	2,500,000	0.6	9.4

It can been seen that the fundamental frequency and amplitude are defining the maximum slew rate in the application and even higher harmonics do not show a higher slew rate as the amplitude is limited. For a DC-DC converter the slew rate is even decreasing because of the $1/\theta^2$ roll-off factor.

With those worst-case calculations, it can be concluded that the maximum slew rate of the current in the application is limited to values of less than 50 A/µs. Any slew rates above 50 A/µs indicate a malfunction or abnormal operating condition and should be considered as a fault resulting in turn-off of the eFuse.

2 Implementation

2.1 Assembly technology

One of the key aspects of the eFuse implementation is the assembly technology. This is the key driver for performance and cost of this solution. In the system, space limits the assembly concept options and therefore different implementation variants are available. These boundary conditions include PCB and assembly technology, manufacturability, cooling strategy, cost, as well as isolation coordination.

The heatsink dimensioning and isolation coordination must be considered together in the design. In a typical application the eFuse could be part of another ECU or an individual ECU (e.g., a power distribution unit). Usually for both options, only convection cooling on the housing of the ECU would be feasible. In this case a galvanic isolation of the heatsink must be included in the design.

For these reasons, the eFuse PoC consists of three different PCBs, as shown in **Figure 9**. The main PCB incorporates all the basic functions, such as gate driver, state-of-health (SOH) diagnosis or output stage protection features. The interface PCB is used to control the demonstrator and supports additional switches for controlling dedicated system tests. On top of the main PCB the output stage is connected to two power connectors and a signal connector.

This way the output stage is exchangeable and different cooling schemes, power levels and technology options are available. The eFuse PoC is designed for a passive cooling system without any fan or liquid cooling. In the next chapters, the two different cooling topologies, top-side cooling (TSC) and bottom-side cooling (BSC), as shown in **Figure 10** will be discussed. For more detailed information please refer to Infineon's application note "Innovative top-side cooled package solution for high-voltage applications" (**AN_2101_PL52_2103_112902**).

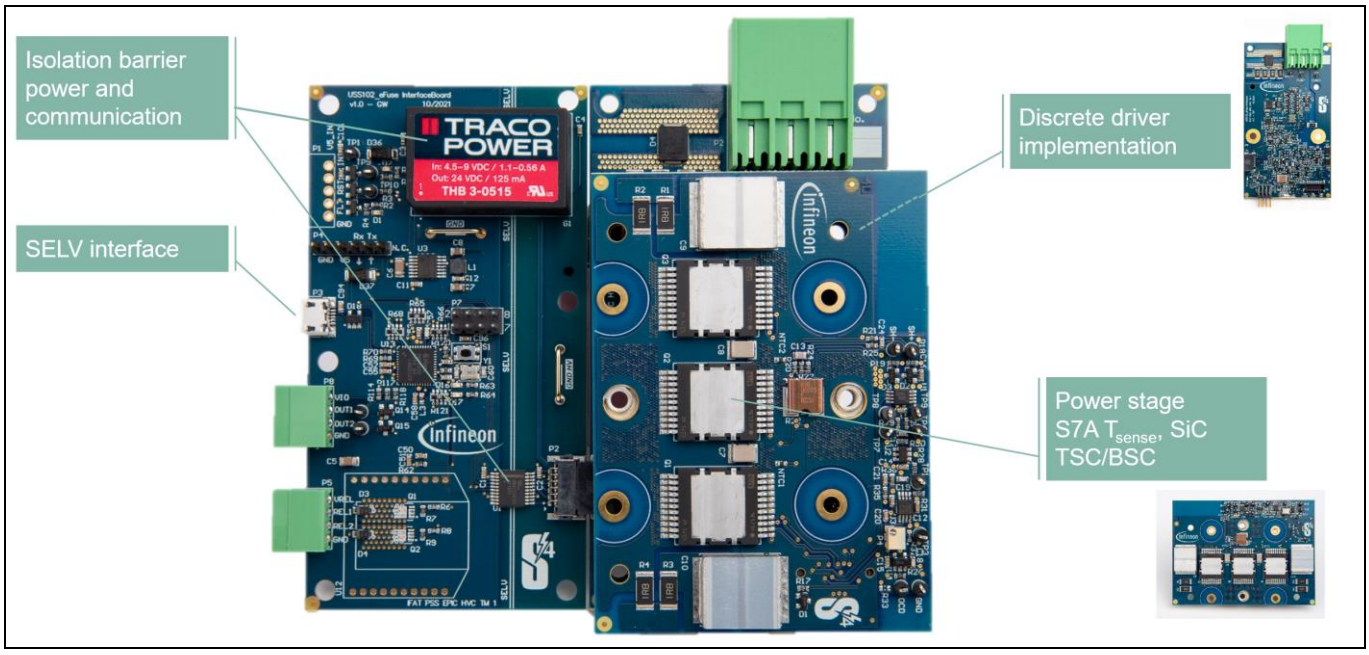

Figure 9 eFuse PoC flexible PCB concept

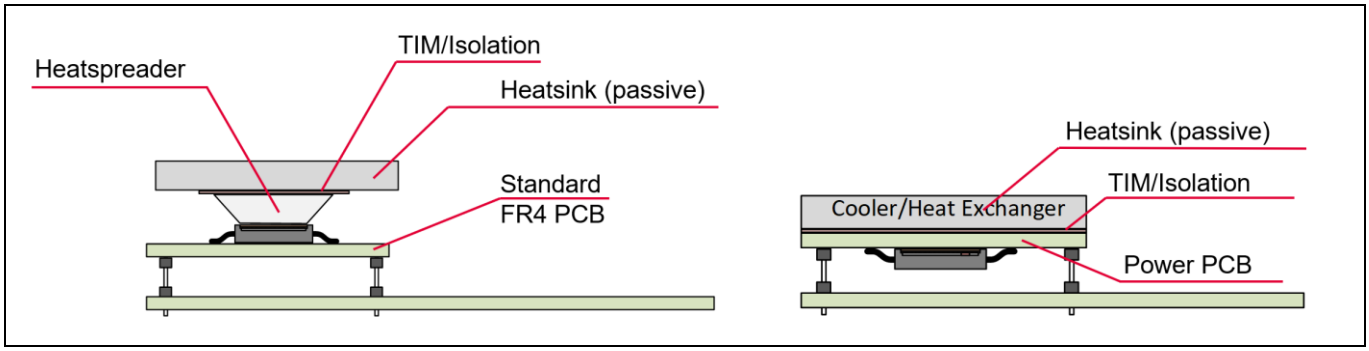

Figure 10 TSC vs. BSC

For the following comparisons, the R_{th} and C_{th} values are calculated with a highly reduced model of each layer using a simplified representation of lateral heat spreading, keeping the vertical dissipation in focus as it is the main contributor for the overall system. In the calculations below, this reduced model for the lateral heat flow would consider a thermal spreading angle of 45 degrees in highly thermally conductive materials. All soldered connections are considered to have a solder void density of 40 percent. For more accurate results, a finite element method (FEM) simulation of the layer stack in the application environment shall be performed.

For comparison reasons, only the R_{th} and C_{th} up to the external cooler are considered in the next chapters, as the main heatsink is dependent on the final assembly concept. In the application the thermal capacitance C_{th} with a very good conductivity to the semiconductor is important for covering short overload conditions, and therefore this is a focus in the upcoming comparisons of cooling concepts.

2.1.1 Top-side cooling output stage

The best cooling performance for the eFuse PoC is achieved with the TSC output stage. In this case, the thermal conduction is separated from the electrical conduction. The thermal losses generated in the semiconductor will be dissipated to the top side of the device and into the external cooling structure, while the electrical energy is conducted through the device pins on the PCB. With Infineon's diffusion soldering die-attach process the thermal resistance from the die to the exposed pad is improved by 40 to 50 percent compared to a soft solder die attach, which results in a minimum R_{th} of the package and an excellent thermal coupling to the heatsink.

To avoid over-dimensioning the power switches to cover the short-term overload patterns in the eFuse application as described in **Chapter 1.4**, the performance of the passive cooling can be significantly improved by applying a heatspreader. When adding thermal capacitance, it is important to consider the isolation coordination strategy, because adding an isolation layer considerably increases thermal resistance, which degrades the efficiency of the applied thermal mass to buffer transient power losses.

The best performance can be achieved by implementing the isolation between the heatspreader and the heatsink. This way, the connection between the heatspreader and the exposed pad can be implemented with a good thermally conductive glue or a solder connection. In addition to the increased thermal mass, the heatspreader is used to increase the interface area in the highly thermally resistive connection to the heatsink.

In **Table 6** and **Table 7** an example calculation, comparing a cooling structure with and without heatspreader, is shown. Even though the heatspreader is an additional series element in the cooling stack, the increase in contact area for the isolating thermal interface material (TIM) significantly decreases the overall R_{th} . The factor 4.8 higher thermal capacity C_{th} with a thermally very good coupling to the device increases the performance of this cooling structure especially for short overload conditions. Furthermore, the main contributor to the overall R_{th} is the TIM towards the heatsink which is needed to compensate for any height differences and positioning tolerances of paralleled devices and includes safe electrical isolation.

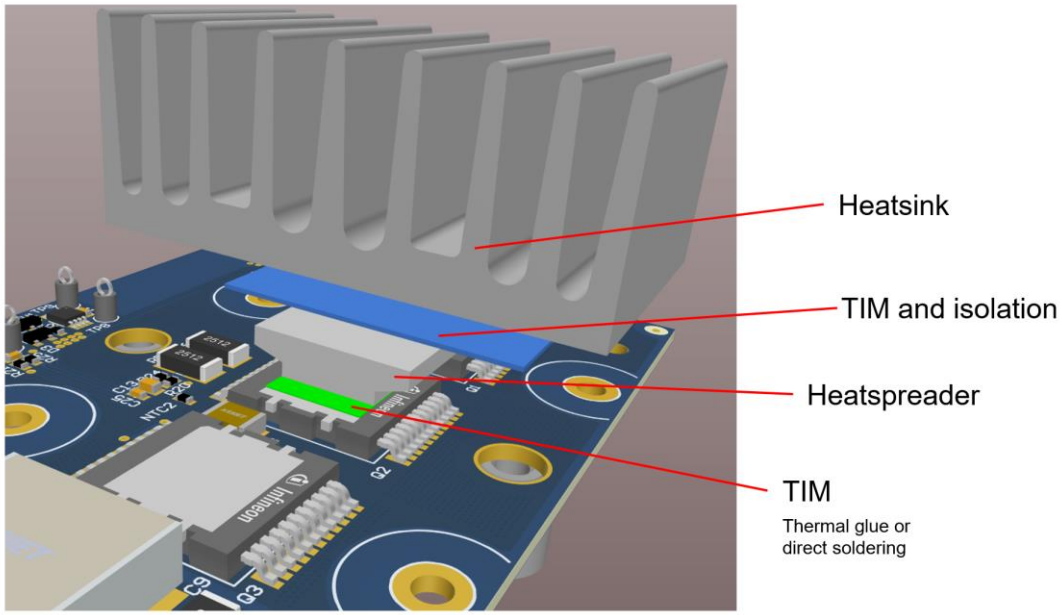

Figure 11 Cooling stackup for eFuse TSC implementation

Table 6 Example stackup for TSC without a heatspreader

	Thickness [µm]	Conductivity [W/mK]	Area [mm²]	R_{th} [K/W]	C_{th} [J/K]
Package	-	-	123.6	0.18	0.379
TIM1 (conductive)	400	3.6	123.6	0.899	-
TIM2 (isolation)	120	1	123.6	0.971	-
Total				**2.05**	**0.379**

Table 7 Example stackup for TSC with a heatspreader

	Thickness [µm]	Conductivity [W/mK]	Area [mm²]	R_{th} [K/W]	C_{th} [J/K]
Package	-	-	-	0.18	0.379
Heat slug solder	100	34.8	123.6	0.023	-
Heatspreader	4500	237	238	0.104	1.458
TIM1 (conductive)	400	3.6	238	0.467	-
TIM2 (isolation)	120	1	238	0.504	-
Total				**1.279**	**1.838**

2.1.2 Bottom-side cooling output stage – standard PCB

For some applications, the assembly concept using a TSC implementation is not feasible. In this case the use of a conventional BSC design is supported by a dedicated package option. The major drawback of a degraded cooling performance is compensated by the benefit of having a standard surface mounted device (SMD) process without the need to allow for different height tolerances of the power devices.

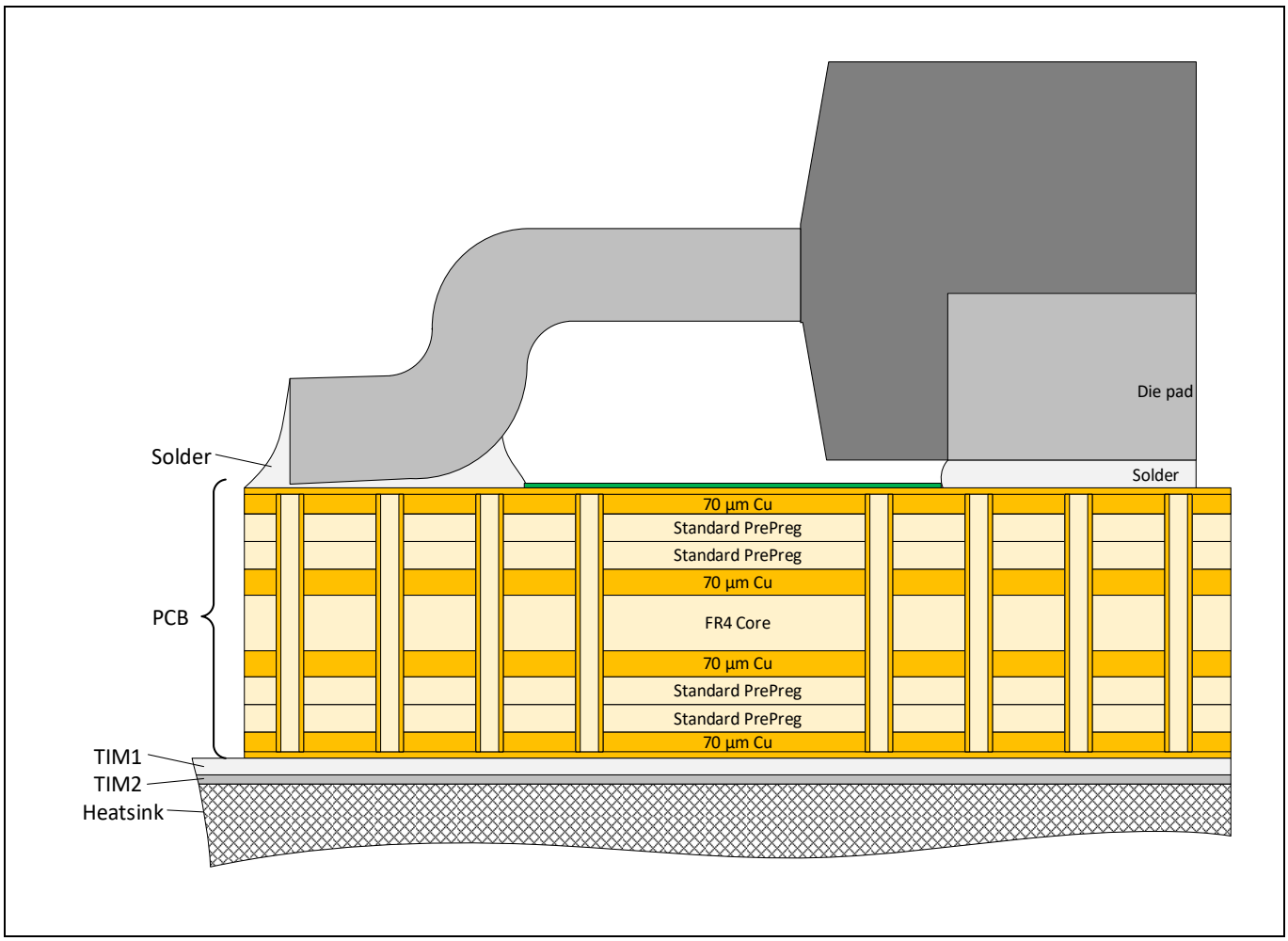

Figure 12 BSC with standard multilayer PCB process

A typical assembly concept based on a standard multilayer PCB process is shown in **Figure 12**. In this case the PCB consists of four 70 µm thick copper layers, separated by FR4 PrePreg or core layers. One of the main disadvantages in a BSC cooling structure is that the thermal energy must be dissipated through the typically ~1.6 mm thick PCB. In order to improve the thermal conductivity of the PCB, filled and capped vias (IPC 4761 Type VII) are placed in high density directly underneath the exposed pad of the device. These vias are placed in a 0.4 mm grid with a drill diameter of 0.2 mm. **Figure 13** shows a potential layer stack of a standard PCB when using a BSC cooling stack. With this stack, the R_{th} and C_{th} can be calculated – see **Table 8**.

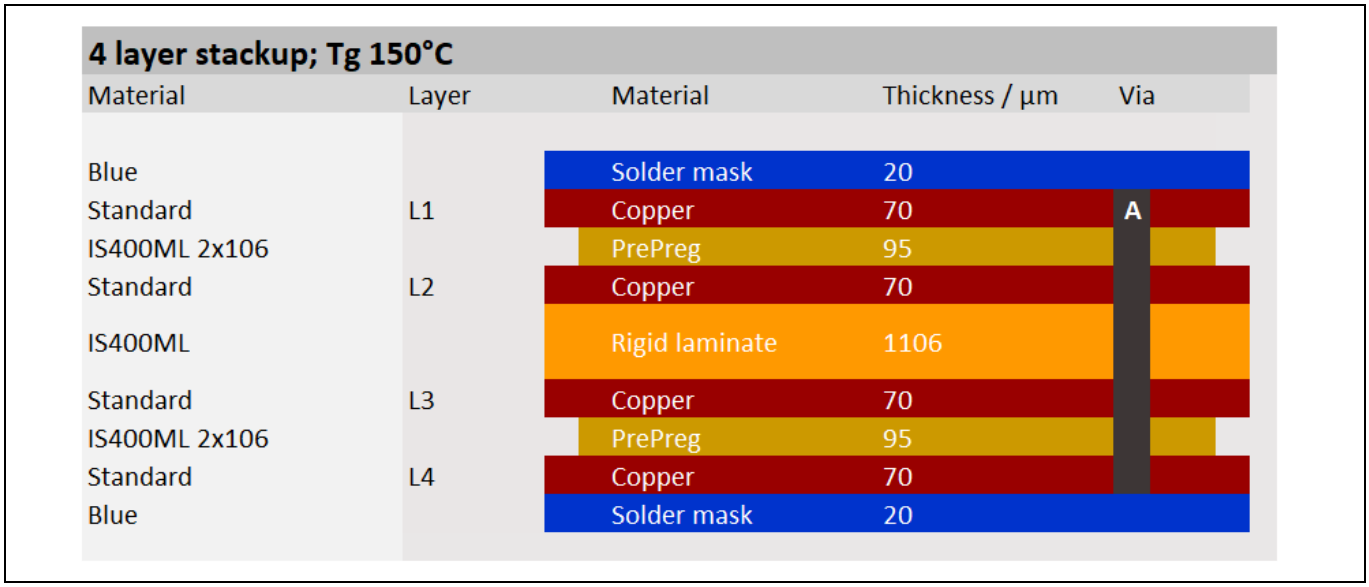

Figure 13 Example layer-stack of a BSC board with standard PCB

Table 8 Example stackup for BSC using a standard PCB

	Thickness [µm]	**Conductivity [W/mK]**	**Area [mm²]**	**R_{th} [K/W]**	**C_{th} [J/K]**
Package	-	-	-	0.18	0.379
Heat slug solder	100	34.8	123.6	0.023	0.042
Top layer	70	399	126	0.001	0.03
PrePreg1 + via	200	15.25	128	0.049	0.002
Inner layer 1	70	399	128	0.001	0.031
Core + via	1200	15.25	130	0.606	0.026
Inner layer 2	70	399	130	0.001	0.031
PrePreg 3 + via	200	15.23	132	0.047	0.002
Bottom layer	70	399	132	0.001	0.031
PCB total	**1680**			**0.911**	
TIM1 (conductive)	300	3.6	238	0.633	
TIM2 (isolation)	120	1	238	0.911	
Total				**2.455**	**0.567**

2.1.3 Bottom-side cooling output stage – advanced PCB

As seen in the previous chapter, the main disadvantage for a back-side cooling solution is the decreased performance of the cooling structure in terms of higher R_{th} and lower C_{th}, which is tightly coupled with the semiconductor. In order to overcome this drawback and still maintain the advantage of maintaining a simpler assembly process, advanced PCB technologies can be used. In this case the significant R_{th} increase due to the FR4 material in the core of the standard PCB can be decreased by the use of a thick copper inlay PCB. Furthermore, superior performance can be achieved if the isolation barrier is moved into the PCB. In this case the PrePreg toward the bottom-side cooler acts as safe isolation barrier, and can be made much thinner compared to an external solution. In this case the TIM toward the heatsink can be electrically conductive, meaning it has higher thermal conductivity than isolating TIM materials.

Implementation

In the power inlay PCB layer stack as shown in **Figure 14**, the top copper layer will be tightly thermally and electrically connected to the thick center layer with filled and capped laser micro-vias (µVias). This tight coupling allows better heat distribution and spreading over a larger surface area, which decreases the thermal resistance to the external heatsink. Another advantage of these thick copper inlay PCBs is that, due to the stiffness of the inner layer, the overall PCB thickness can be reduced, as well as the thickness of the TIM compensating for mechanical tolerances (e.g., PCB bending).

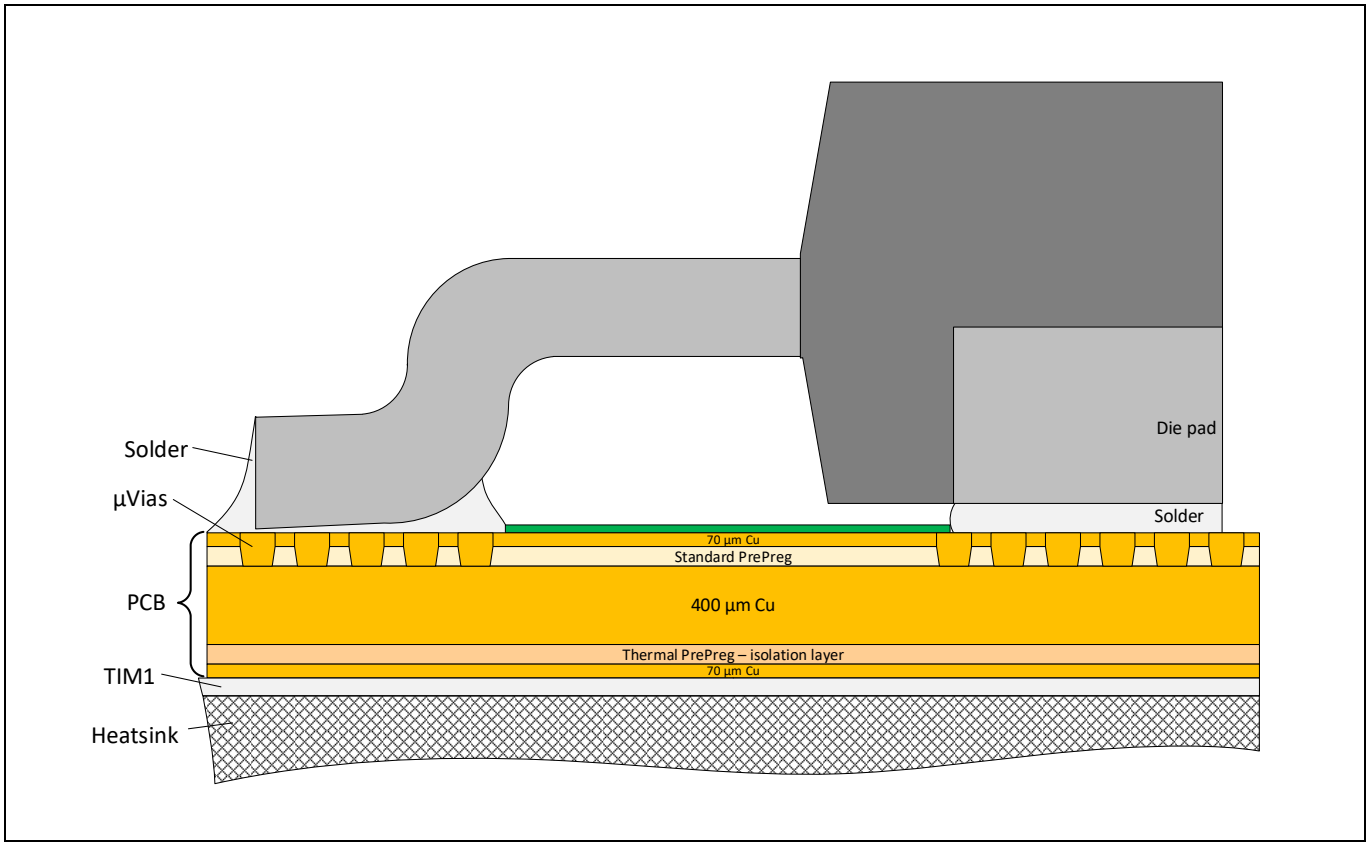

Figure 14 Example layer stack of an inlay PCB

Table 9 Example stackup for BSC using an advanced PCB process

	Thickness [µm]	**Conductivity [W/mK]**	**Area [mm²]**	**R_{th} [K/W]**	**C_{th} [J/K]**
Package	-	-	-	0.18	0.379
Heat slug solder	100	34.8	123.6	0.023	0.042
Top Layer	70	399	126	0.001	0.03
PrePreg1 + via	95	15	128	0.049	0.002
Inner layer	70	399	129	0.008	0.175
PrePreg 2 (special)	95	1.3	140	0.527	0.002
Bottom Layer	70	399	140	0.001	0.033
PCB total	**870**			**0.789**	
TIM1 (conductive)	200	3.6	140	0.401	
Total				**1.19**	**0.663**

2.1.4 Bottom-side cooling output stage – isolated back side

As discussed in **Chapter 2.1.3,** to simplify assembly the isolation layer is moved inside the PCB. In order to reduce the cost of an advanced PCB process, an isolation scheme can also be used with a standard power PCB process. Even though the thermal resistance and capacitance are degraded compared to the other implementations, this assembly concept may give the best performance-per-cost ratio.

In this case the backside of the PCB is already isolated and the PrePreg 3 is used for the safe isolation towards the cooling structure. The thermal performance calculation is shown in **Table 10**. In order to improve the thermal performance, instead of using a standard FR4 material for the PrePreg, a higher performance thermal PrePreg should be used. This significantly increases the cooling performance of the cooling stack, as this layer is the main contributor to the total R_{th}. **Figure 15** shows an example layout of the eFuse PoC output stage with high-density, filled µVin the exposed pad.

Table 10 Example stackup for BSC with isolated backside

	Thickness [µm]	Conductivity [W/mK]	Area [mm²]	R_{th} [K/W]	C_{th} [J/K]
Package	-	-	-	0.18	0.379
Heat slug solder	100	34.8	123.6	0.023	0.042
Top Layer	70	399	126	0.001	0.03
PrePreg1 + via	200	15.25	128	0.049	0.002
Inner layer 1	70	399	128	0.001	0.031
Core + via	1200	15.25	130	0.606	0.026
Inner layer 2	70	399	130	0.001	0.031
PrePreg 3	200	0.36	132	2.004	0.002
Bottom Layer	70	399	132	0.001	0.031
PCB total	**1770**			**2.867**	
TIM1 (conductive)	300	3.6	238	0.633	
Total				**3.49**	**0.567**

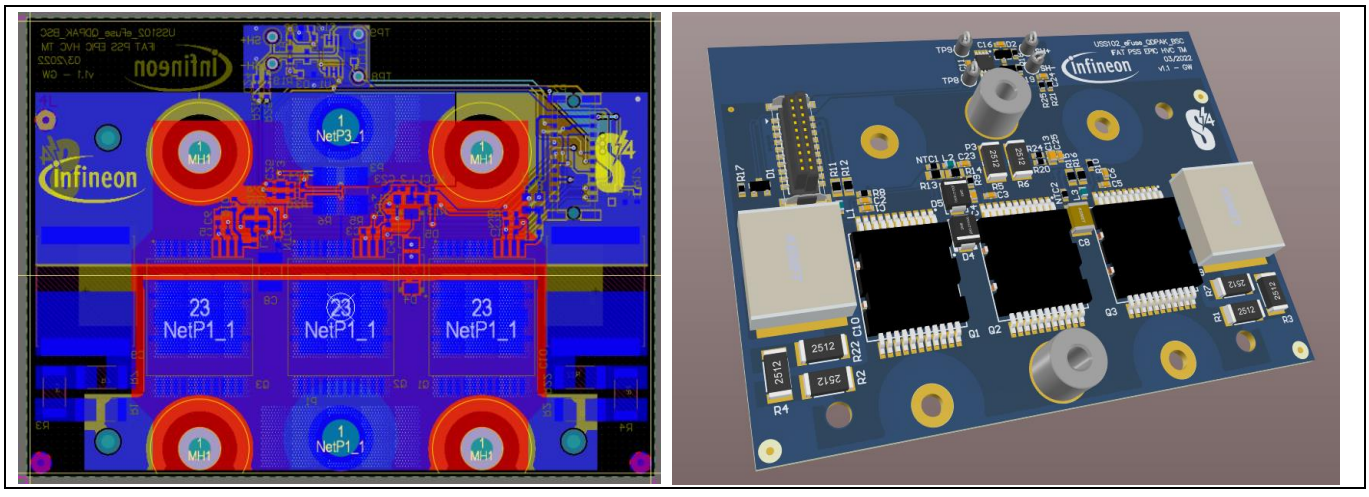

Figure 15 Example layout of the eFuse PoC output stage

2.1.5 Comparison of TSC vs. BSC

For all implementation concepts, the isolation layer is the main contributor for the R_{th}. In the BSC cooling structure implementation the PCB's FR4 material, especially the core in the center, is an additional major contributor, even though the thermal conductivity is already improved with thermal vias directly in the exposed pad. To overcome this drawback in the BSC cooling performance, it would be possible to use a special PCB technology (e.g., inlay process) to achieve a similar cooling performance as with the TSC approach.

Table 11 and **Table 12** shows a comparison of the R_{th} and C_{th} for the different power stage implementations. In **Figure 16** the R_{th} and C_{th} contributors for the different implementation options are displayed. With this representation, for example, in the TSC implementation both TIMs contribute equally to the total R_{th} and are the best choice for further improvement. The comparison of the thermal capacitance only shows the low-ohmic connected thermal mass, as this is key for supporting short overcurrent pulses. The main contributor to the thermal capacitance is the external heatsink which needs to be isolated and is therefore less effective for those short-term overloads.

With all cooling and assembly schemes discussed, a comparable thermal performance can be achieved. Depending on the implementation, an advanced assembly process (TSC) or a higher cost PCB back-side cooling concept can be selected.

Table 11 Comparison of R_{th}

R_{th} [k/W]	**TSC without heatspreader**	**TSC with heatspreader**	**BSC Standard PCB**	**BSC Advanced PCB**	**BSC Standard isolated**
PCB/heat slug solder	0.18	0.203	0.911	0.789	2.867
Heatspreader	-	0.104	-	-	-
TIM1 (conductive)	0.899	0.467	0.633	0.401	0.633
TIM2 (isolation)	0.971	0.504	0.911	-	
Total R_{th}	**2.050**	**1.279**	**2.455**	**1.190**	**3.500**

Table 12 Comparison of thermally low-ohmic coupled C_{th}

C_{th} [J/K]	**TSC without heatspreader**	**TSC with heatspreader**	**BSC Standard PCB**	**BSC Advanced PCB**	**BSC Standard isolated**
Heat slug	0.379	0.379	0.379	0.379	0.379
PCB	-	-	0.188	0.283	0.188
Heatspreader	-	1.458	-	-	-
Total C_{th}	**0.379**	**1.838**	**0.567**	**0.663**	**0.567**



Figure 16 Distribution of the R_{th} and C_{th} contributors for different assembly options

2.1.6 Thermal model

For all the different assembly schemes a thermal FEM simulation has been performed. For simple verification and testing of different load patterns, a Cauer network has been created for each cooling structure. These Cauer networks can be used in any SPICE simulator and give a good indication of how the cooling structure is performing. **Figure 17** shows an example of such a Cauer network used in electro-thermal SPICE simulations. On the MOSx terminals, the junction temperature terminal of the L3 SPICE model of the MOSFETs are connected and with the BASE terminal the ambient temperature is set. The T_j node of the Infineon MOSFET model refers to the junction temperature of the power device as a voltage node (1V ≡ 1°C) and a current of 1 A would represent 1 W of power intake (for more information see AN2014-02). **[3]**

Figure 18 shows the use of the Cauer model in a simplified power model. In this simulation three IPDQ60R010S7A devices are used in parallel and connected to the thermal model. The starting temperature is defined with a voltage source and to consider the additional power losses of the shunt resistor on the center MOSFET, an additional current source has been added. The ambient temperature of the heatsink is set with a voltage source connected to the Cauer model. In this simulation the R_{th} of the external heatsink is adjusted to the one which was used in the application by adding an additional resistor at the HS output of the model.

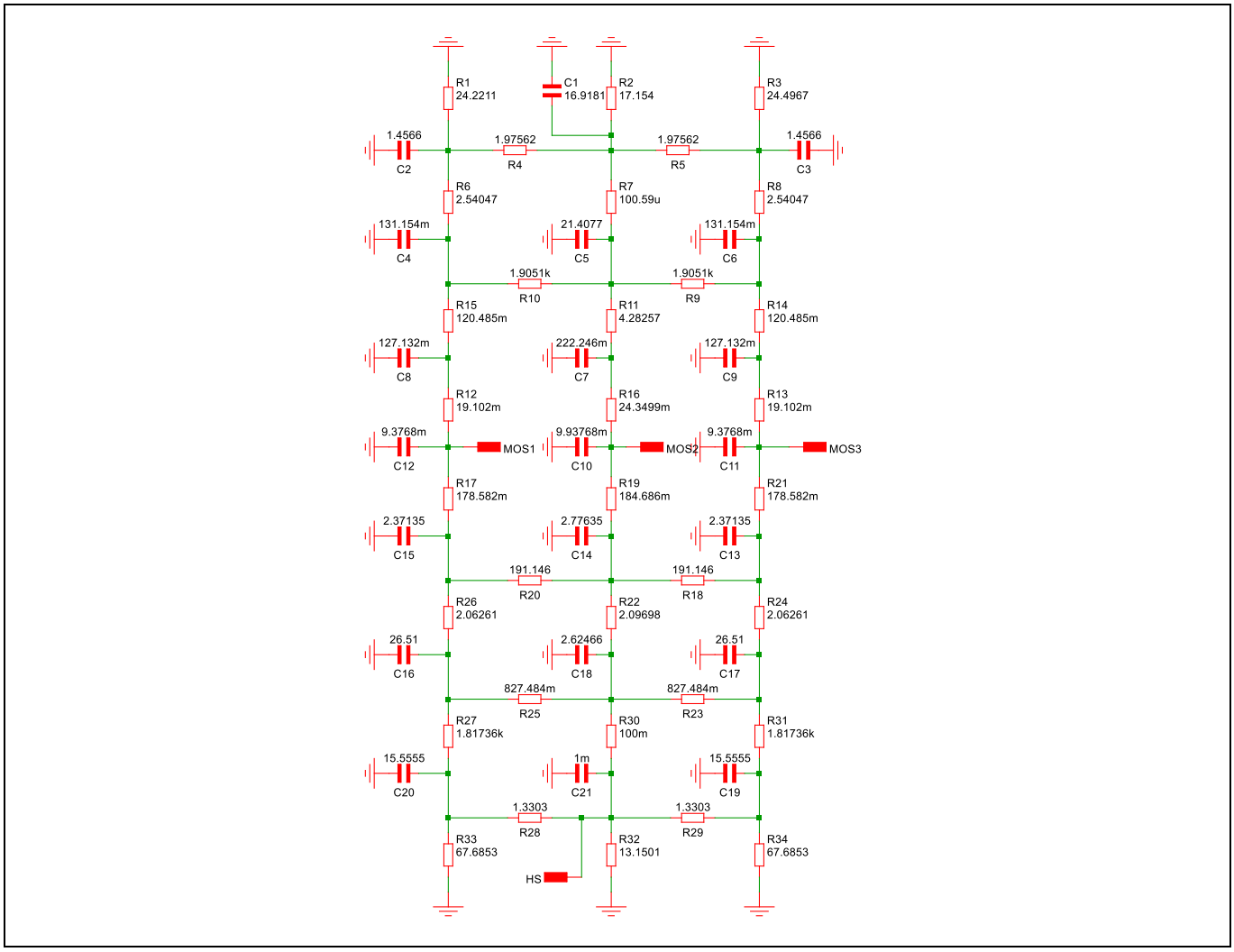

Figure 17 Cauer network of TSC with heatspreader

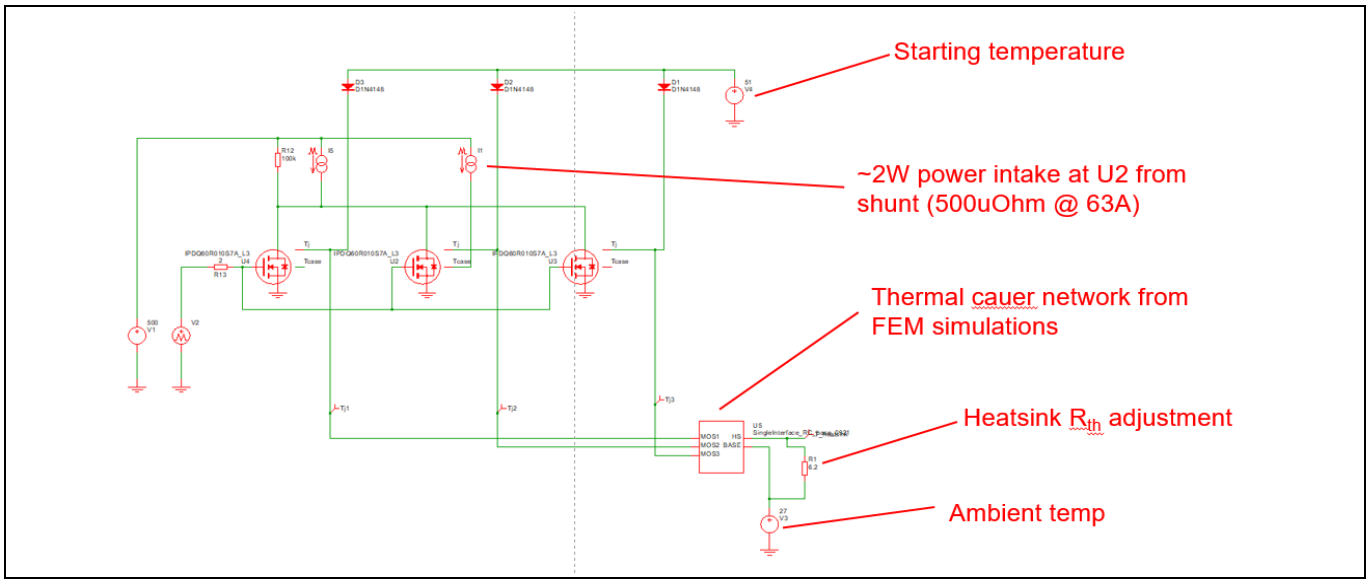

Figure 18 Use of Cauer network in an electro-thermal SPICE simulation

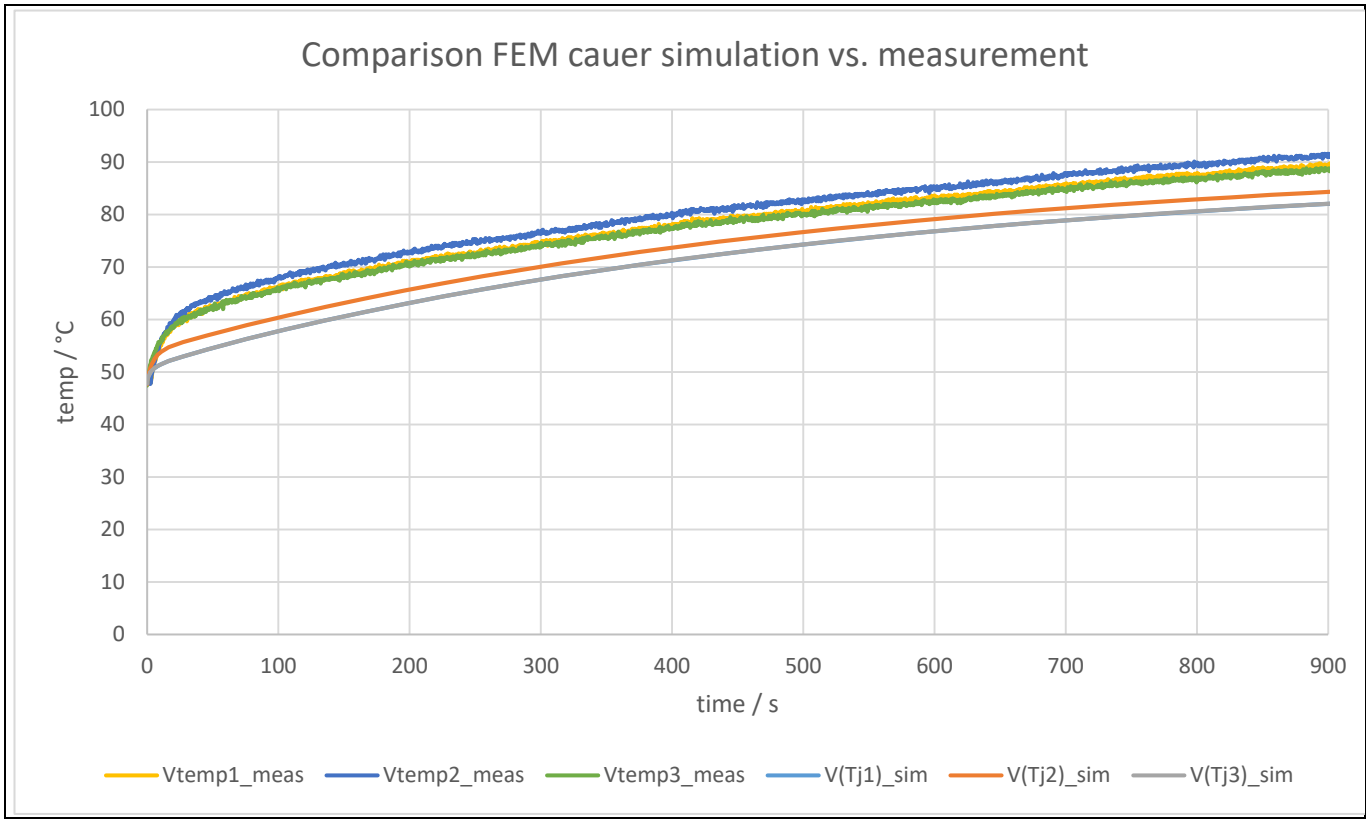

Figure 19 Measurement vs. simulation results

2.2 Diagnostic and protection concept

In static switch applications such as an eFuse the integrity and reliability of the power semiconductor is essential, as any failure in the power device could result in a catastrophic and potentially hazardous condition for the end-user. With their excellent manufacturing and high-quality gates, Infineon's MOSFETs have a very low failure probability. Nevertheless, this reliability is only ensured if the device is operated in the specified operating range. Stress factors which affect the reliability and lifetime of semiconductors include high temperature, fast temperature gradients, overvoltages, and overcurrents.

To ensure the integrity of the power stage, the eFuse PoC incorporates an advanced safety, diagnostic, and protection concept. This protection concept includes:

- Power MOSFET thermal protection
- Device cooling supervision
- Redundant and diverse overcurrent protection (OCP)
- Overload detection
- Built in self-test (BIST) system for power device SOH diagnostics
- System voltage supervision

2.2.1 Overtemperature protection

As predominant failure mechanisms in a semiconductor are triggered through overtemperature or temperature gradients, an output stage in safety relevant applications should be dimensioned conservatively. This will lead to an over-dimensioning of the output stage and will not result in a cost-effective design. This chapter discusses appropriate measures in order to ensure a safe operation of the eFuse with a progressive- and cost-minimized design of the output stage.

Abnormal operating conditions, e.g., overcurrents due to failures in the load or wiring harness, can lead to a thermal overloading of the eFuse power stage which would in turn result in damage to the output stage if no protection mechanism is in place. In order to protect the output stage from these critical conditions, measurement of the power device die temperature is essential.

There are multiple options to implement a temperature sensing scheme in the application. A cost-sensitive solution is to use the observer method, where the die temperature is estimated indirectly with respect to other operating conditions (e.g., load current, ambient temperature, cooling structure …). With this method, the estimation error is dependent on the accuracy of the observer model in the current operating point. In that case any changes in the system due to e.g., degradation effects or errors of the input variables will have an impact on the temperature sensing accuracy. This error must be taken into consideration when dimensioning the output stage and therefore for a cost-effective design a more accurate sensing method is key.

Any direct temperature information which is located closer to the actual semiconductor will improve the accuracy of such observers significantly and can be realized in various ways, as shown in **Figure 20**.

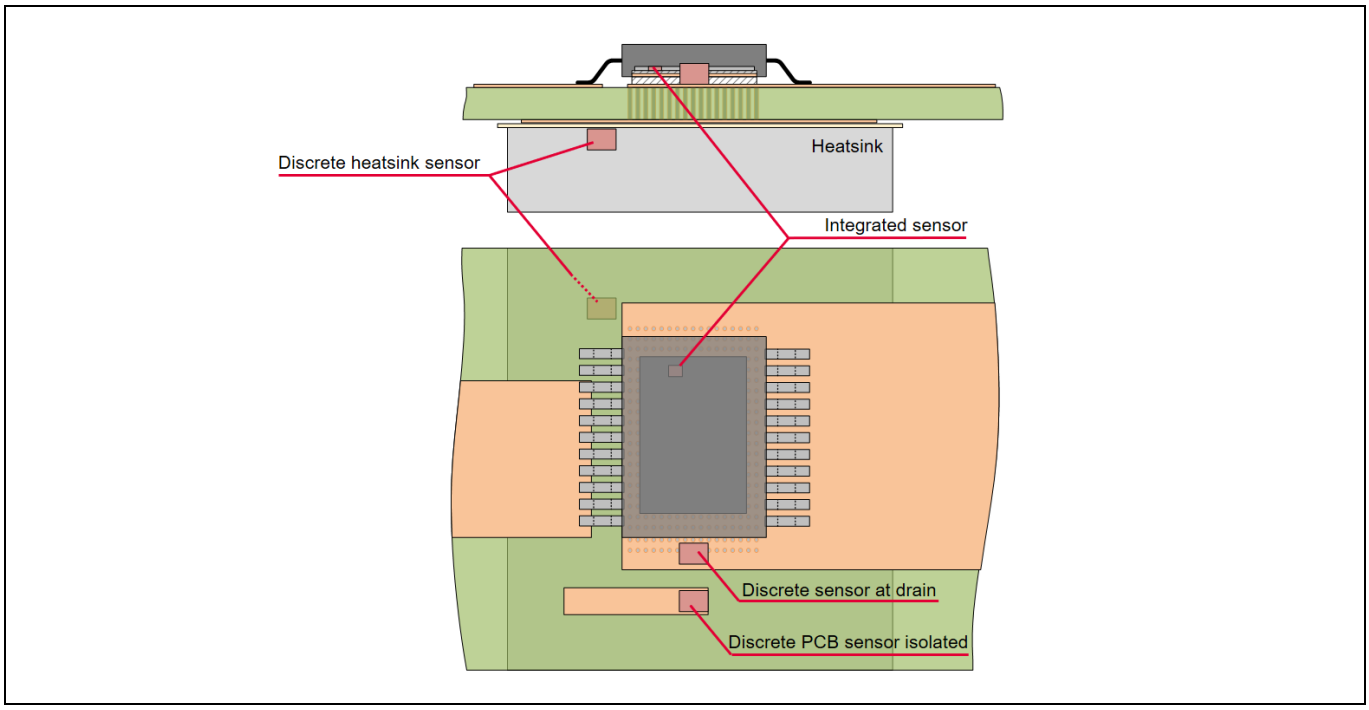

Figure 20 Different possible temperature sensing positions

Discrete sensor at drain:
When using a vertical power semiconductor technology, the current flow from drain to source is in the vertical direction. In this case the drain potential is on the back of the chip, which is soldered onto the exposed pad of the package. This exposed pad is on the drain potential and due to the solder connection is thermally well coupled to the chip. In this case using a discrete temperature on the drain potential gives a good representation of the die temperature and because of the tight thermal sensor coupling the measurement delay of temperature transients is reasonably low. In HV applications, this implementation has the drawback that the temperature evaluation must be referenced to the drain potential of the power device and therefore a HV evaluation circuit is needed.

Discrete PCB sensor, isolated:
In this case a discrete temperature sensor, which is isolated from the power device potential, is used to measure the PCB temperature. This simplifies the evaluation circuitry as the temperature sensor is galvanically isolated from the HV potential. However, the thermal coupling to the actual die temperature is limited because the only physical connection is through the PCB base material, in which thermal conductivity is a factor of ~1000 less than copper. This introduces very slow feedback of the die temperature information and a low-pass effect with a high time constant, where short current pulses and the corresponding temperature transients are not detectable by the sensor. This type of implementation could be used as an ambient temperature sensor as an input for an observer method, as this method includes a drop in the junction temperature.

Discrete heatsink sensor:
The temperature sensor is embedded in or attached to the external heatsink. In this case the sensor is thermally tightly coupled with the external heatsink but depending on the implementation has a limited coupling to the junction temperature as the heatsink is isolated from the HV potential of the power device as discussed in **Chapter 2.1**. This implementation includes a high delay and a drop of the temperature measurement and leads to problems with fast transients, and therefore this implementation can be used as an additional input for an observer method.
Another challenge with this solution is that the sensor is now externally and galvanically isolated from the power electronics which makes implementation and connection to the control unit more difficult.

Integrated sensor:
A direct, monolithic integration of the temperature sensor gives the best thermal coupling and lowest delay time of all sensor implementations. It is referenced to the source potential of the power device which is used by the gate control circuitry and therefore an isolation is not needed to read out the sensor.

It is a direct measurement of the die-temperature which does not rely on any other measured variables or complex behavioral models and furthermore any tolerances or failures in the assembly have no impact on the accuracy of the measurement. Because of that, the integrated sensor can be used to detect delamination or degradation of the cooling stack during the lifetime of the system.

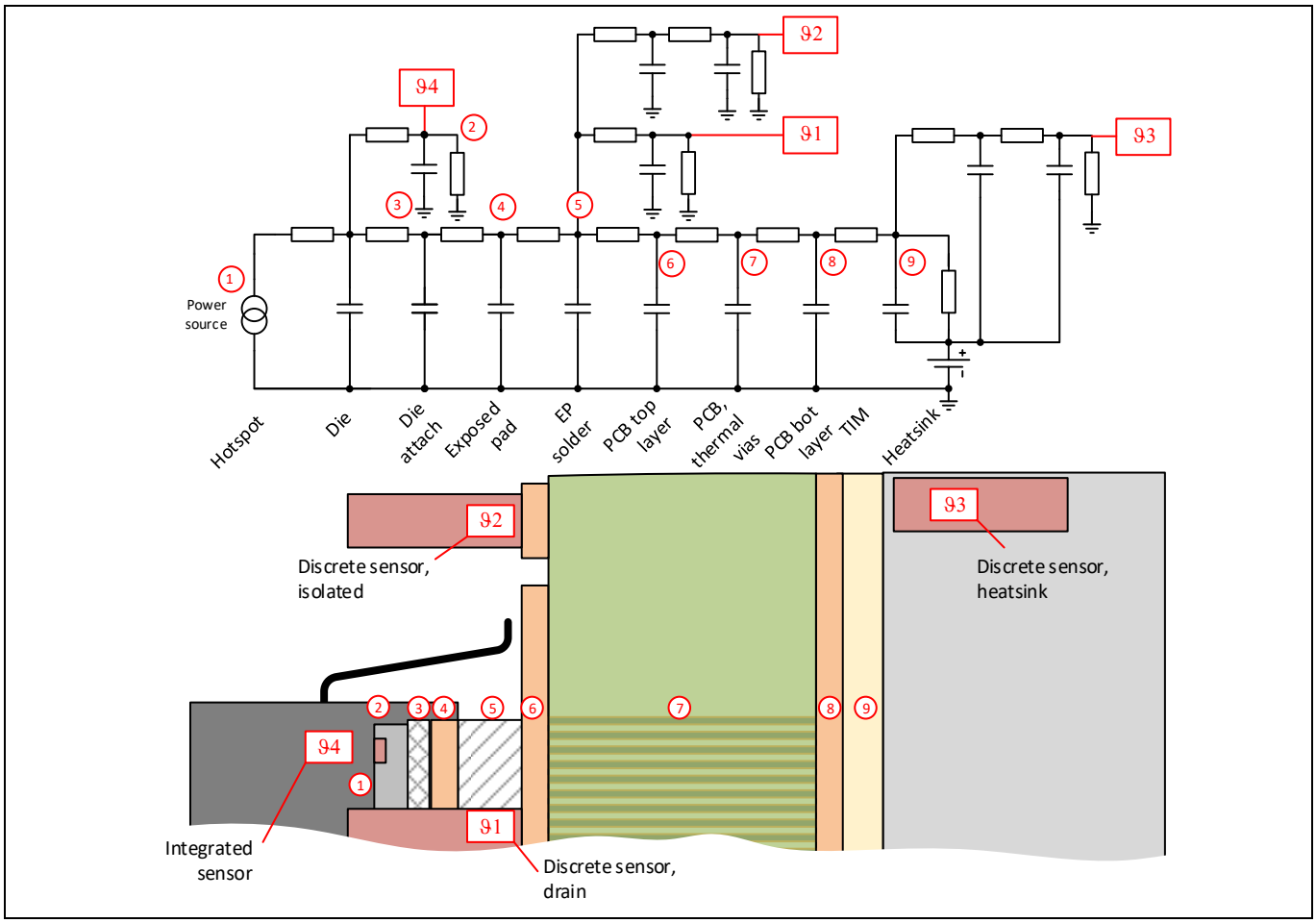

Figure 21 Simplified thermal model of different temperature sensing location

The benefits and disadvantages of different sensing implementations in terms of delay and response time can be seen in the simplified thermal model in **Figure 21**. Each of these thermal resistance and capacitance elements introduces an additional damping of the amplitude as well as a time delay of the measured temperature. With an observer solution using discrete temperature sensors, this RC network needs to be precisely characterized to determine the threshold margins in the application. All tolerances in the complete signal chain need to be considered when dimensioning the power stage, resulting in a conservative device utilization.

In addition to that, observer solutions rely on the integrity of several input parameters (e.g., ambient temperature, current measurements, voltage measurements) and a failure in one of those measurements would also result in an error in the observer. In this case, for safety-relevant applications, the observer with all input parameters should be implemented according to the functional safety requirements. Furthermore, all

series elements from the temperature sensor toward the hotspot contribute to the failure probability of the system.

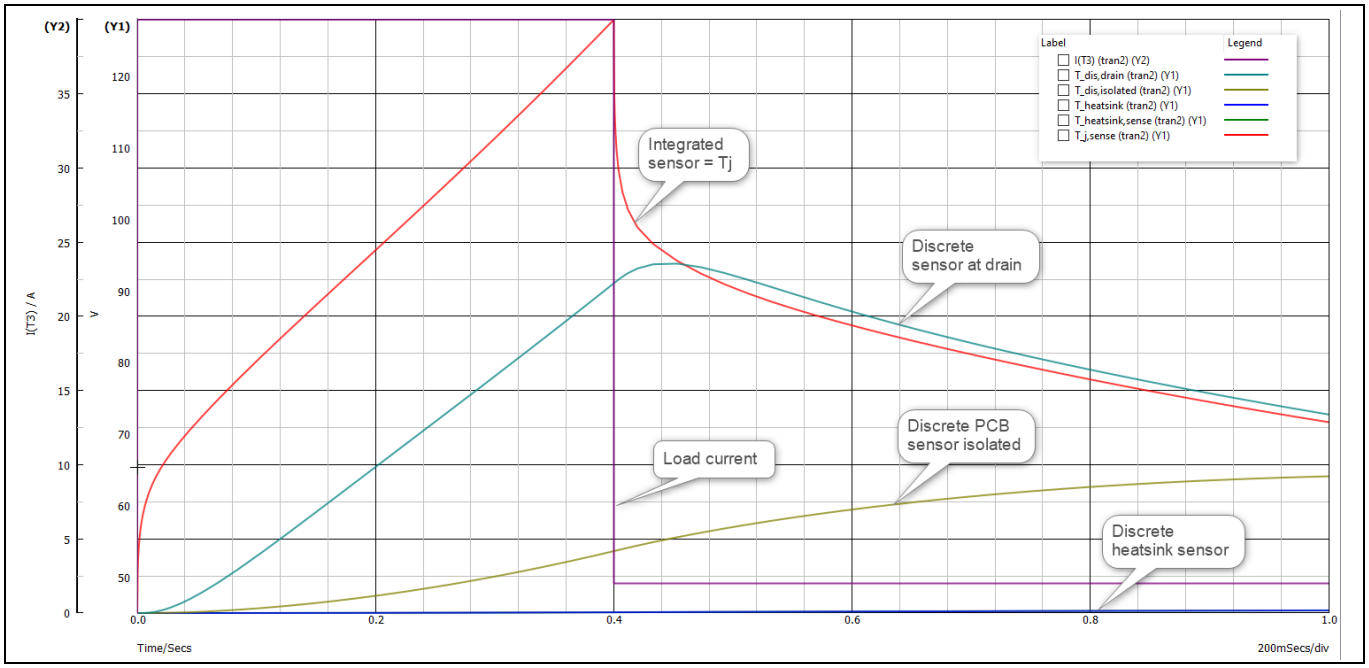

Figure 22 Simulation result of different temperature sensing locations

Figure 22 shows a simulation result of the simplified model shown in **Figure 21** with the different sensing locations for a 400 ms current pulse. The different time constants of the sensor locations are showing that for short current pulses only an embedded sensor can be used to protect the power device without the need for an additional observer.

In summary there are several benefits of implementing the sensor on the die compared to any observer-based solution:

- Direct measurement of die temperature with minimized delay and response time
- Independence of cooling structure
- Discrimination of individual power devices possible when paralleling
- Detectability of thermally disconnected, degraded or damaged devices from the heatsink
- Better utilization of the power device as a minimal safety margin is needed

The eFuse PoC incorporates Infineon's CoolMOS™ IPDQ60T010S7A power device, which features an embedded temperature sensor and can provide the die temperature information individually on a dedicated pin. The temperature sensor is implemented as a series connection of three diodes to increase the sensitivity over temperature. A typical temperature characteristic of the sensor voltage V_{temp} for a given bias current and the principal schematic of the device is shown in **Figure 23**.

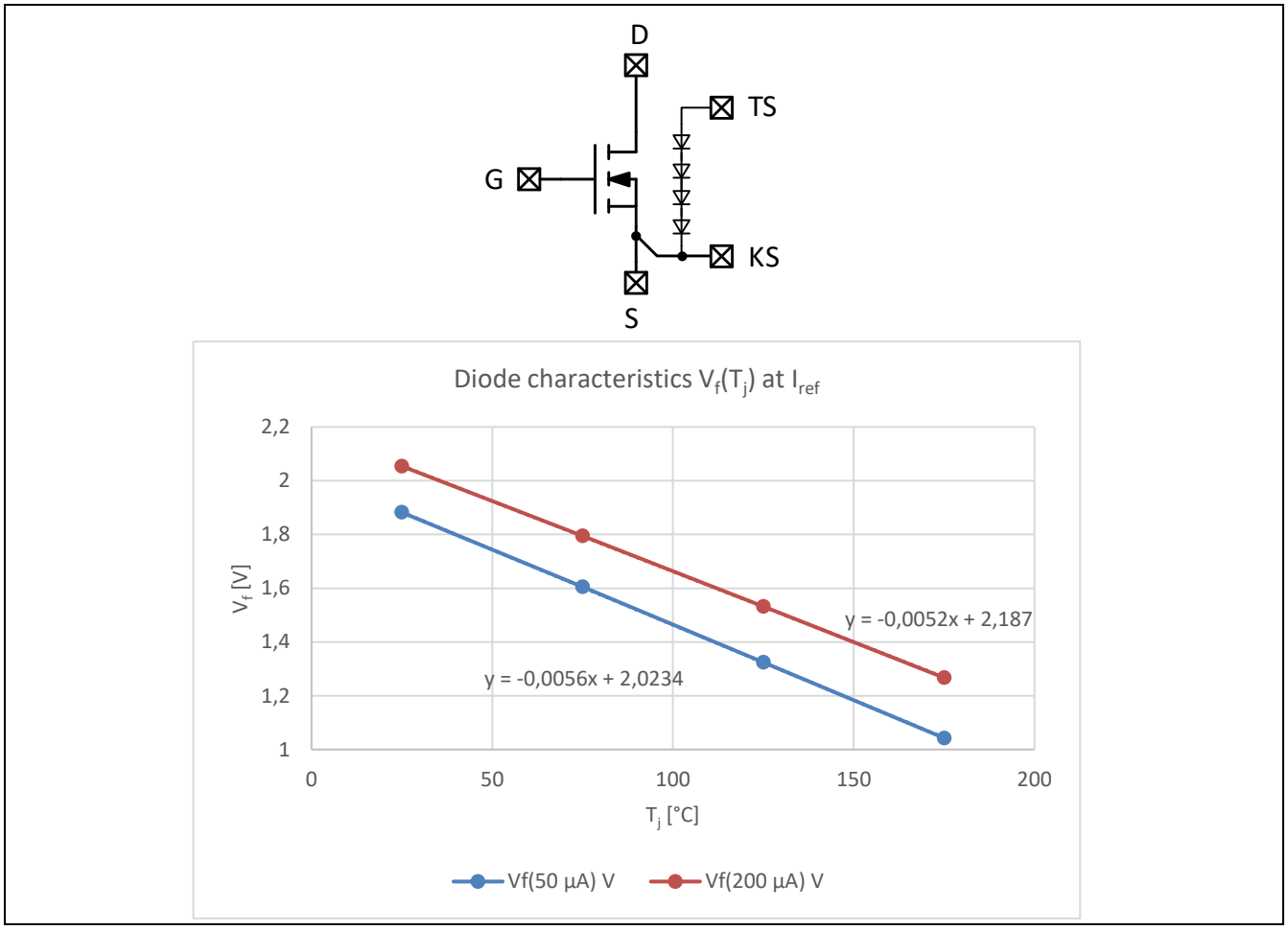

Figure 23 Schematic of the power device and typical V_{temp} dependency over temperature

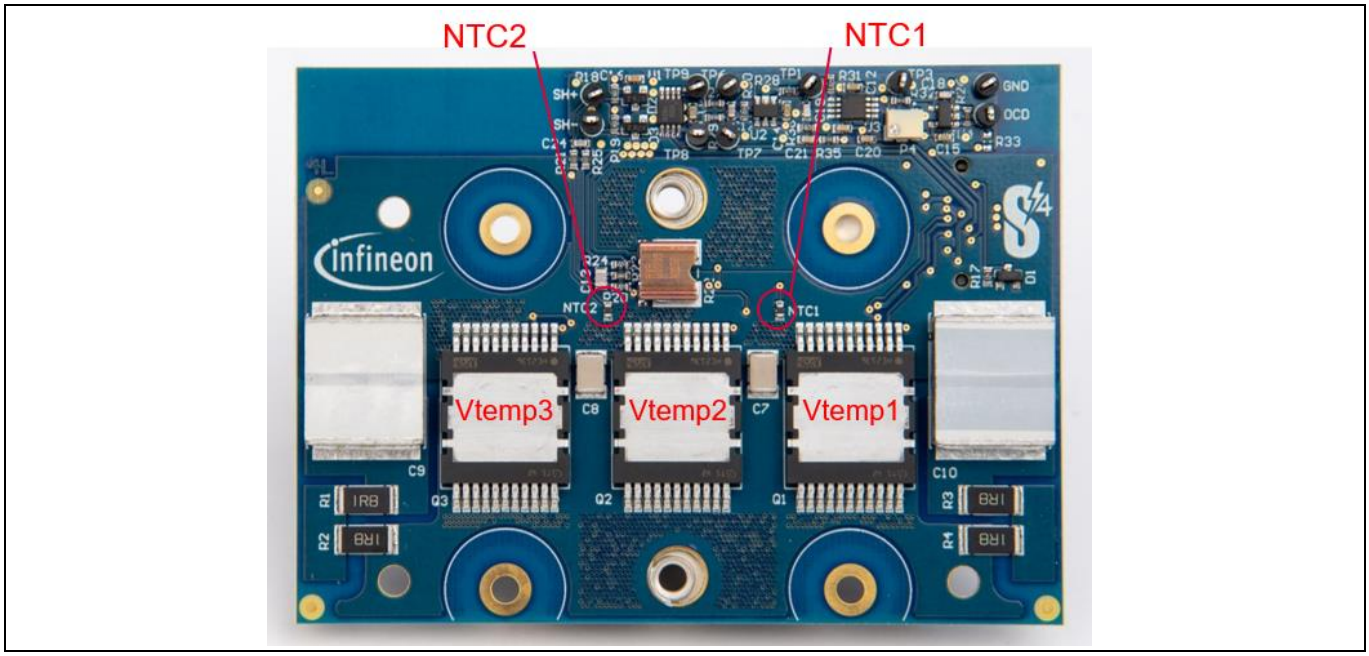

Figure 24 Location of on-die and discrete temperature sensors on the PoC

Implementation

A time-multiplexing scheme of the bias current is used to read out the on-die temperature sensors in the eFuse PoC. This multiplexing allows the readout of the sensors individually with the need for only one current source and analog infrastructure (signal conditioning, ADC inputs) of the control unit. **Figure 25** shows the readout principle of the on-die temperature sensors in the eFuse PoC.

As discussed in **Chapter 1.3**, the thermal protection of the output stage is needed in case of overload or overcurrent events which do not trigger the OCD. The power stage of the eFuse is dimensioned so that it can withstand currents below the overcurrent shutdown for more than 10 ms. In the PoC an update rate of ~200 Hz is achieved with the embedded sensing principle, and this is fast enough for a thermal shutdown. Additionally, the overtemperature warning and overtemperature shutdown are software configurable. The biasing current for the diode stack used in the eFuse PoC is 200 µA.

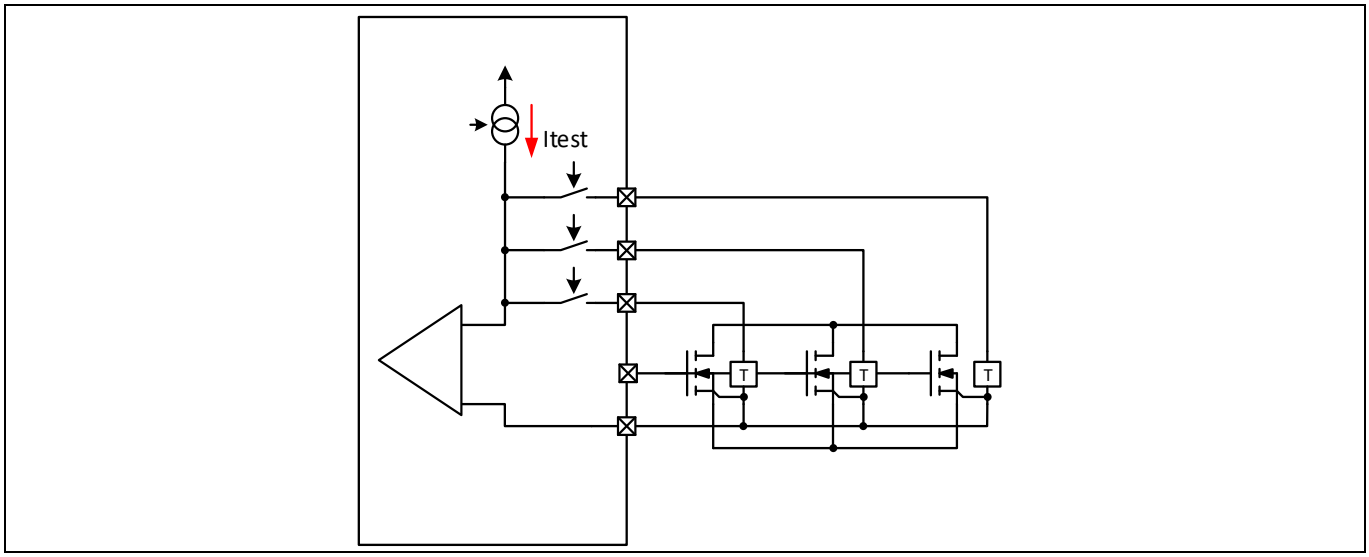

Figure 25 Readout principle of the on-die temperature sensors

The eFuse PoC incorporates two different temperature sensing methods for comparison. **Figure 24** shows the position of the three embedded and two discrete negative temperature coefficient (NTC) temperature sensors. As the performance of the embedded sensors are better than the discrete solution, they are used for the thermal shutdown of the power stage.

The discrete NTC temperature sensors are connected to the source potential of the power MOSFETs, which simplifies the measurement circuitry, as the electronic control is also referenced to the source potential and can be used as input for a redundant and diverse observer method. The biasing current for the NTC temperature sensor is generated with a pull-up resistor in series to the NTC. This results in a non-linear transfer characteristic of the temperature vs. the NTC voltage as shown in **Figure 26**. The calculation of the temperature can be realized with a fitted polynomial calculation or a lookup table to save computing power.

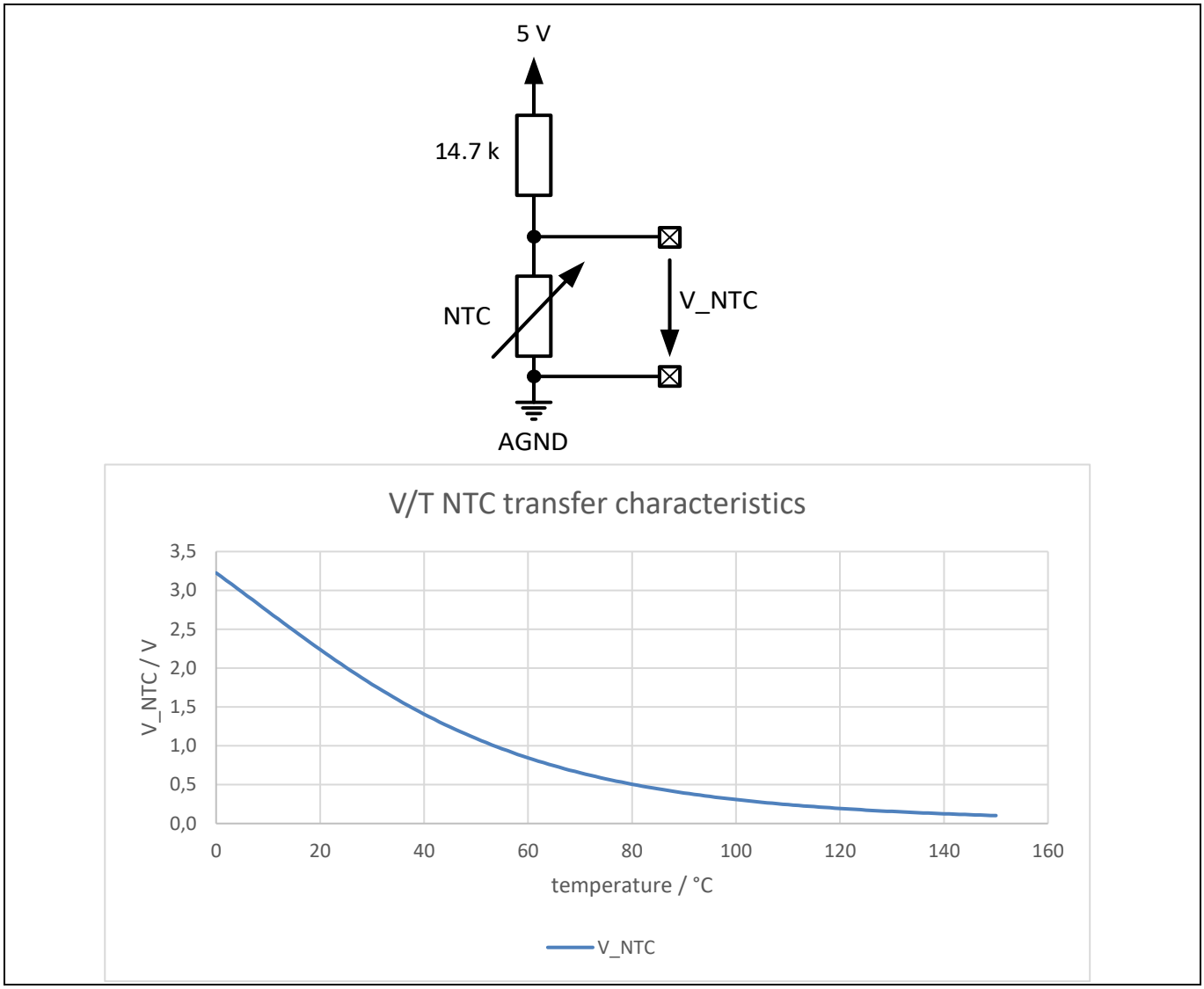

Figure 26 NTC characteristics with pull-up resistor

2.2.2 Overcurrent patterns – short circuit profiles

In a typical application, a variety of different external faults can lead to an overcurrent event in the eFuse. A protected auxiliary load could be a drive application (e.g., HVAC-compressor) or any other load controlled with an inverter output stage (e.g., on-board charger (OBC), heater). Potential external failures that could lead to different overcurrent scenarios are shown in **Figure 27**.

Potential failures in the auxiliary load include output wiring short, failure in the power stage, an inverter control failure (shoot-through), a stuck motor or a failure in the bulk capacitor. Furthermore, the wiring harness to the auxiliary load is another potential point of failure and it can be differentiated between load short circuits and terminal short circuits in the auxiliary cable. The main difference between these two short circuit types is the residual impedance of the wiring harness, resulting in a difference of the current slew rate and clamping energy requirement.

When evaluating all these different failure cases, faults in the load can be covered as a load short circuit in perspective of the eFuse and therefore, only the terminal short circuits and load short circuits cases are going to be differentiated further.

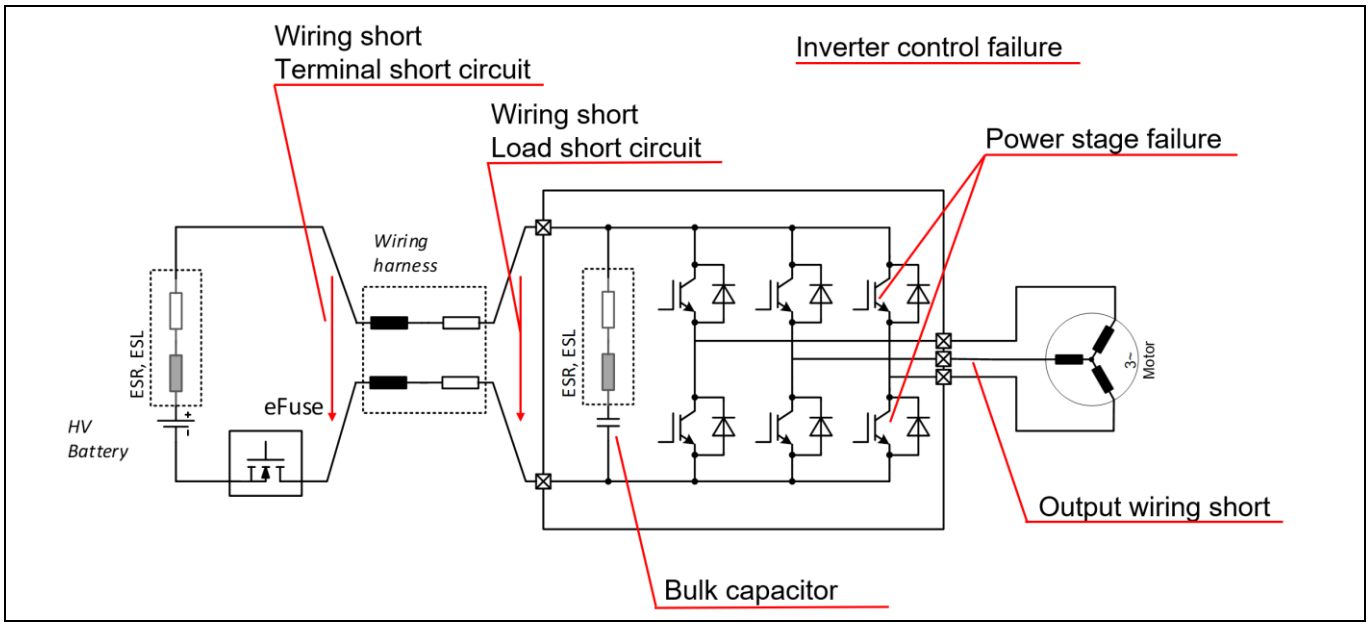

Figure 27 External faults which lead to overcurrent events in the eFuse

When considering the typical boardnet topology for a centralized eFuse application as discussed in **Chapter 1.3**, the protected auxiliary branch is in a parallel connection to the main inverter. The current slew rates as well as the clamping energy in short circuit conditions depends on the wiring harness and the boardnet topology and therefore the requirements change depending on the system architecture.

Typical minimum cable lengths from the power distribution box to the main inverter are ~0.5 m, and to the auxiliary inverter ~1 m. The battery to the junction box and internal wiring of the junction box is considered to be at least ~0.5 m long. The HV battery is assumed to have a series inductance of 17 µH, the current measurement shunt in the eFuse is 3 nH and for the wiring harness an inductance of 1 µH/m is considered.

Load short circuit:
The equivalent schematic diagram for a load short circuit event is shown in **Figure 28**. In a short circuit condition the limiting factor for the current slew rate is the inductance of the system and the short circuit itself. The resistive part of the impedance is in this case too low to effectively limit the current and can be taken out of consideration. The system is in normal operating mode before the short circuit event and all DC-link capacitors

are charged up to the battery voltage. For the duration of a short circuit event these capacitors represent a low impedance energy source and can be paralleled in the equivalent schematic with the battery. The short circuit itself is considered with a parasitic inductance of 1 µH.

The total short circuit inductance is ~3.9 µH in this case. The main current contributor to the short circuit current is the DC-link capacitor of the main inverter, as the ESL of the capacitor and the wiring harness is significantly smaller than the series inductance of the HV battery. The maximum slew rate in this configuration is calculated as follows:

$$\left(\frac{di}{dt}\right)_{max,LSC} = \frac{V_{bat}}{L_{total}} = \frac{500\ V}{3.9\ \mu H} = 128.2\ {}^{A}/_{\mu s}$$

As discussed in **Chapter 1.4**, the OCD limit needs to be set to a value of more than 110 A. It is therefore necessary to implement a high-speed OCD circuit to limit the overshoot and as a result the clamping energy which needs to be handled by the eFuse during turn-off. With a detection delay of 300 ns and the previous calculated slew rate this would result in a clamping energy and switch-off power of:

$$I_{shutdown} = I_{OCD} + I_{overshoot} = 110\ A + 38.46\ A = 148.46\ A$$

$$P_{LSC} = U_{bat} \cdot I_{shutdown} = 500\ V\ \cdot 148.46\ A = 74.2\ kW$$

$$E_{LSC} = \frac{1}{2} L_{total} \cdot I_{shutdown}^2 = \frac{1}{2} 3.9\ \mu H \cdot 148.46^2 A^2 = 42.98\ mJ$$

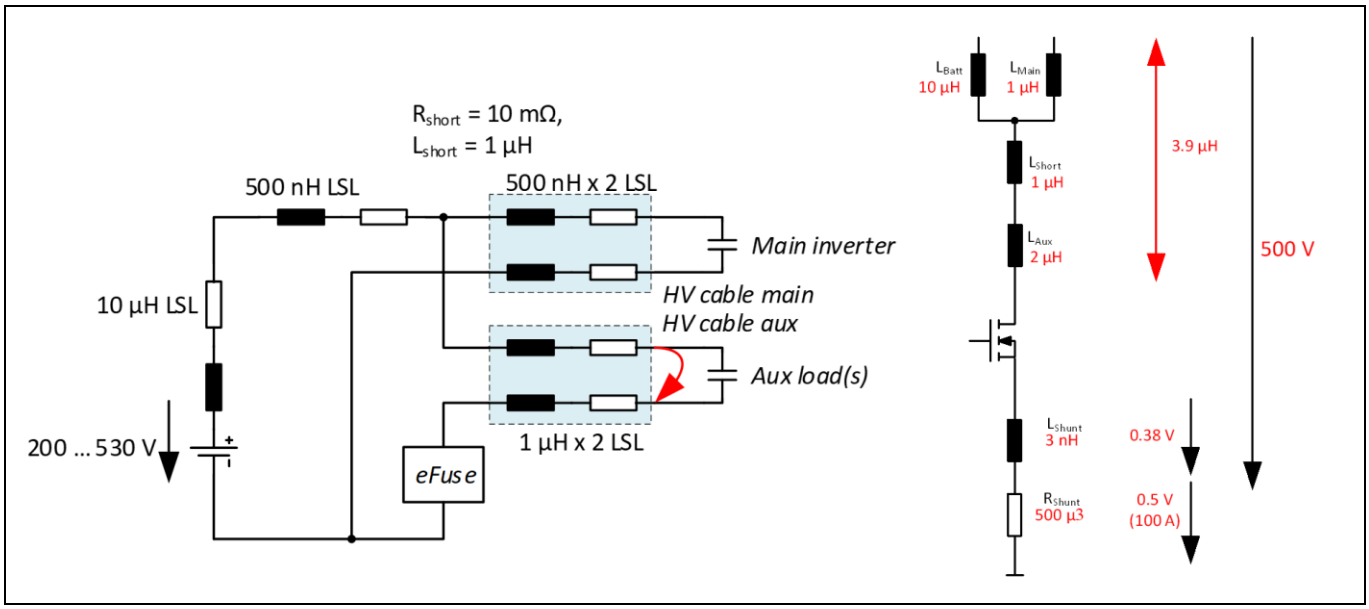

Figure 28 Equivalent schematic diagram for a load short circuit

Terminal short circuit:

Figure 29 shows the equivalent circuit diagram for a terminal short circuit. The equivalent circuit diagram is similar to the LSC case but in this case the bulk capacitor of the auxiliary inverter is additionally contributing to the short circuit current in the eFuse. Due to this lower total short circuit inductance, the current slew rate is higher than in the LSC case and more dependent on the short circuit inductance:

$$\left(\frac{di}{dt}\right)_{max,TSC} = \frac{U_{bat}}{L_{total}} = \frac{500\ V}{1.6\ \mu H} = 312.5\ {}^{A}/_{\mu s}$$

The shutdown current, power and clamping energy are calculated as follows:

$$I_{shutdown} = I_{OCD} + I_{overshoot} = 110\ A + 93.75\ A = 203.75\ A$$

Implementation

$$P_{TSC} = U_{bat} \cdot I_{shutdown} = 500\ V\ \cdot 203.75\ A = 101.87\ kW$$

$$E_{TSC} = \frac{1}{2} L_{total} \cdot I_{shutdown}^2 = \frac{1}{2} 1.6\ \mu H \cdot 203.75^2 A^2 = 33.2\ mJ$$

To prevent excessive current overshoot and high clamping requirements, a high-speed detection circuit (t_d less than 300 ns) is necessary. Furthermore, the short circuit inductance plays a major role in the terminal short circuit and the clamping energy is lower than in a load short circuit. The influence of a higher shutdown delay or lower short circuit inductance can be seen in **Table 13**:

Table 13 Terminal shutdown parameters with different delay times and short circuit inductance

	L_{short} = 1 µH			L_{short} = 500 nH		
	$(di/dt)_{max}$ = 312.5 A/µs			$(di/dt)_{max}$ = 454.5 A/µs		
t_{delay} [us]	$I_{shutdown}$ [A]	$P_{shutdown}$ [kW]	E_{clamp} [mJ]	$I_{shutdown}$ [A]	$P_{shutdown}$ [kW]	E_{clamp} [mJ]
0.3	203.75	101.88	33.21	246.36	123.18	33.38
0.5	266.25	133.13	56.71	337.27	168.64	62.56
1	422.5	211.25	142.81	564.55	282.27	175.29
1.5	578.75	289.38	267.96	791.82	395.91	344.84

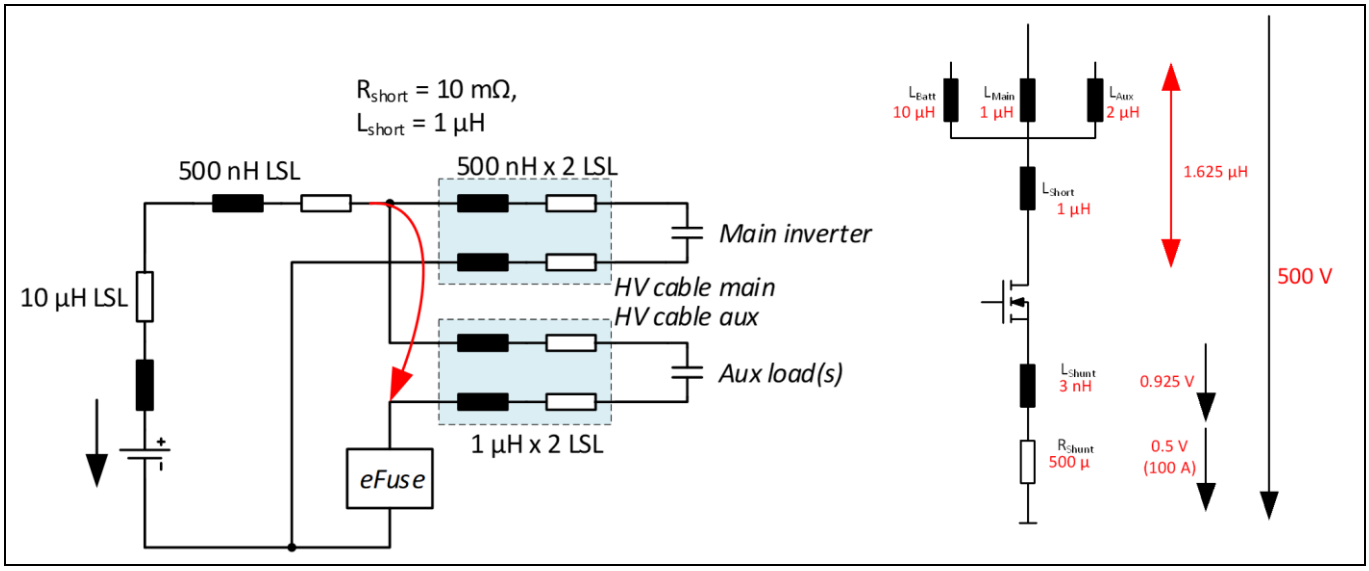

Figure 29 Equivalent schematic diagram for a terminal short circuit

2.2.3 Overcurrent protection

Even though the on-die temperature sensors already give a very fast and accurate feedback on the die temperature, fast OCD is essential for comprehensive protection of the output stage. Especially during very fast and short overcurrent pulses, e.g., short-circuit, the response time of the temperature sensor is too slow to protect the output stage effectively.

As a fast and reliable OCD is required for the protection of the power stage in failure conditions, a redundant and diverse detection method may be necessary to cover functional safety related application requirements. As shown in **Figure 30**, in the eFuse PoC a V_{DS}-based current sensing scheme is implemented as an alternative or redundant concept to the shunt solution.

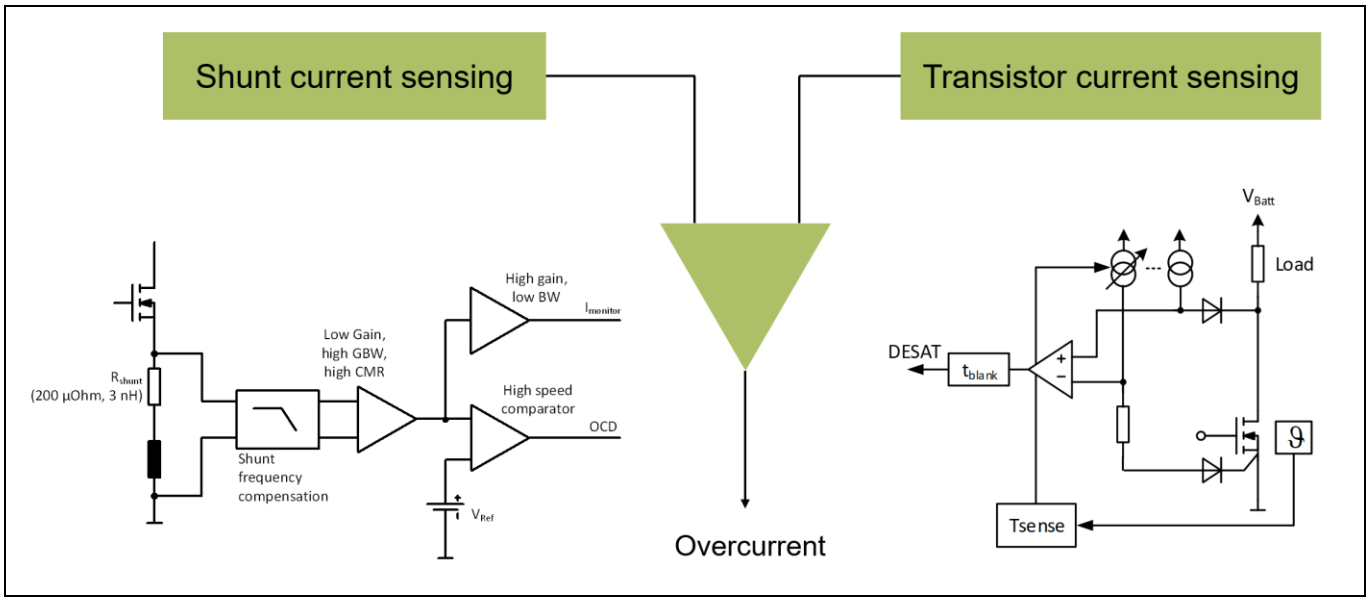

Figure 30 Redundant and diverse OCD scheme

Shunt based overcurrent detection:
The most common way to sense a current is by using a shunt resistor in the power path and measuring the voltage drop across this resistor. In the eFuse PoC the shunt-based measurement is used for monitoring the current through the eFuse as well as protecting the power devices in case of overcurrent events. As discussed in the previous chapter, the OCD delay should not exceed 300 ns in order to prevent excessive overshoots in case of low-impedance short circuit events.

The drawback of using a shunt resistor to implement a high-speed measurement is the parasitic inductance of the resistor. A typical high-power shunt has a series inductance of approximately 3 nH **[2]**. This results in a high-pass frequency response with the corner frequency:

$$R_s = \omega_c L = 2\pi f_c L_s$$

$$f_c = \frac{R_s}{2\pi L_s}$$

Lower shunt values result in a lower corner frequency of the measurement. For a 200 µΩ shunt resistor with a parasitic series inductance of 3 nH, the corner frequency would be at 6.4 kHz. This high-pass behavior would lead to a measurement error in the frequency region above 6.4 kHz resulting in a decreased OCD threshold.

When now comparing this frequency response with the spectrum of typical loads in an eFuse application (see **Chapter 1.5**) the high-pass behavior of the shunt resistor could lead to a false OCD when a ripple current of an

inverter or DC-DC converter load is present. The overlap in the amplitude spectrum is shown in **Figure 31**. In this example a switching frequency of 10 kHz for the inverter and 100 kHz for the DC-DC converter with the typical power ratings as discussed in **Chapter 1.4** is considered.

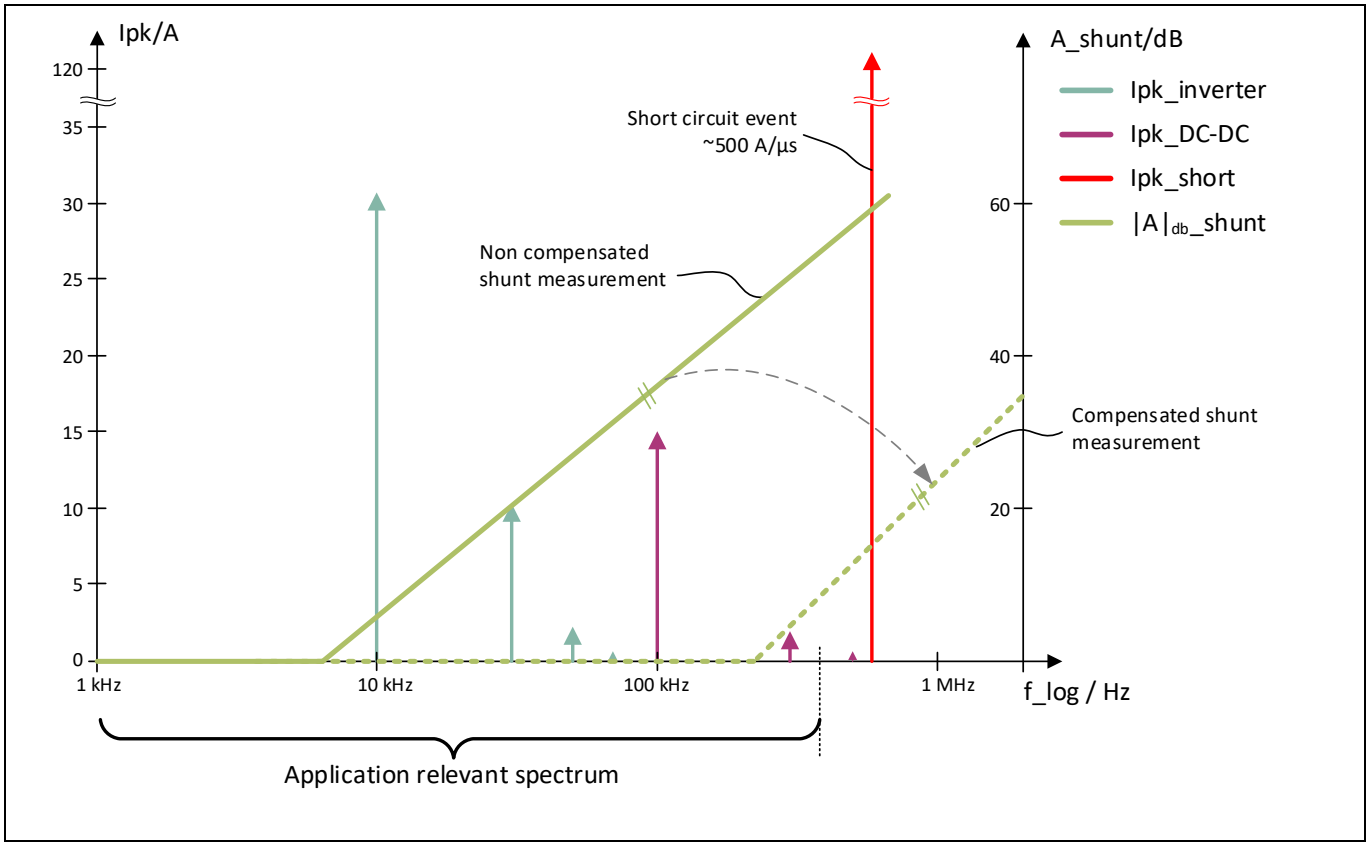

Figure 31 Typical load amplitude spectrum and shunt frequency comparison

For a constant OCD, the high-pass frequency response of the shunt resistor must be compensated and the corner frequency should be shifted to higher frequencies outside the dominant spectrum of the application as shown in **Figure 31**. This can be done in different ways – one option would be to reduce the parasitic inductance of the shunt resistor by selecting a different shunt or parallel configuration, or to compensate it with additional signal conditioning. However, when dimensioning the signal conditioning, it could be beneficial to maintain a high-pass behavior in the frequency region above the application-relevant spectrum. In this case, the OCD threshold would be decreased for transients above the application relevant slew rates of more than 50 A/µs and this would reduce the overshoot in abnormal operating conditions (e.g., short circuit).

In the eFuse PoC the compensation for the high-pass behavior is done in several ways. First the parasitic inductance of the shunt is reduced by using two low-inductive shunt resistors in parallel configuration. Then the shunt resistor value is increased to 500 µΩ which increases the corner frequency. Finally, a two stage low-pass filter as shown in **Figure 32** is implemented to compensate for the remaining high-pass behavior in the application-relevant spectrum. A simulation result of the two stage low-pass filter and the operational amplifier stage is shown in **Figure 33** (estimated parasitic shunt and wiring inductance of 3 nH). With this filter the OCD threshold behavior for higher slew rates can be adjusted. The overcurrent switch off threshold characteristics in the eFuse PoC is shown in **Figure 34**.

A typical turn-off measurement using the shunt-based OCD in a load short circuit is shown in **Figure 35**, with a current slew rate of 83 A/µs. In this case the inductive effect of the shunt resistor can be seen in the $V_{shunt,ampl}$ signal. The total delay from detection until the switch-off is approximately 300 ns.

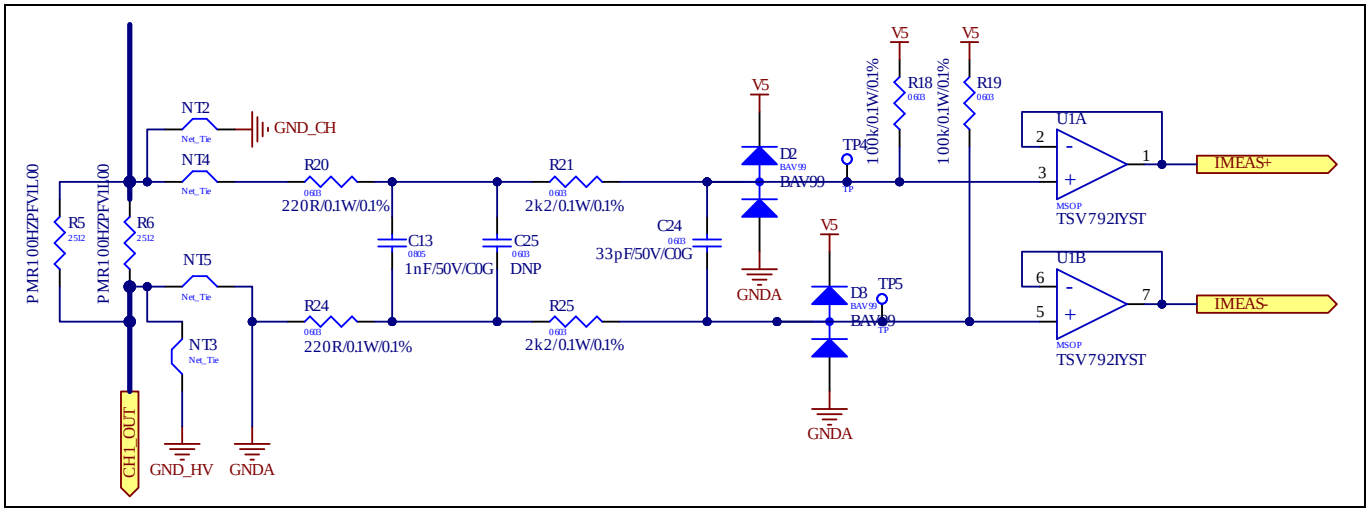

Figure 32 Frequency compensation filter for shunt measurement

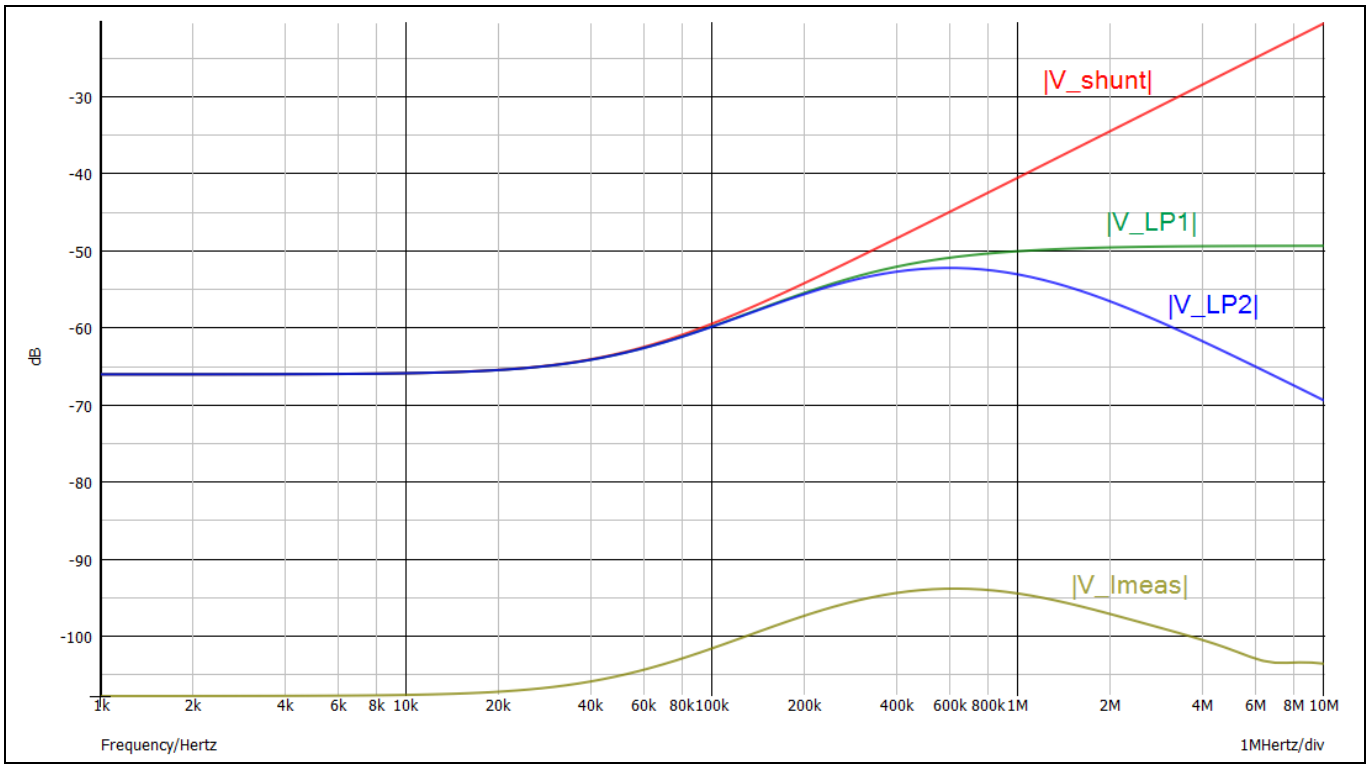

Figure 33 Simulated amplitude response of implemented current measurement compensation

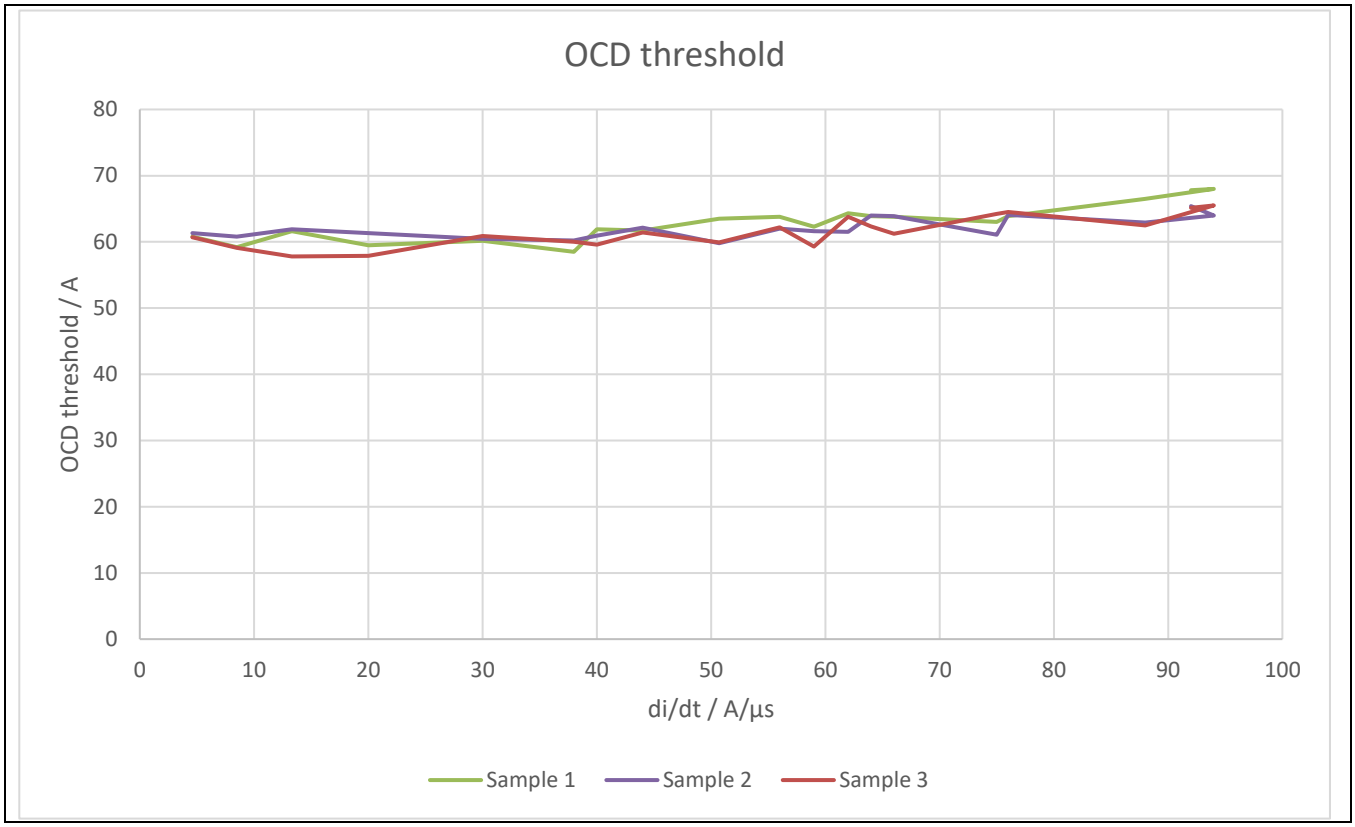

Figure 34 Measurement of optimized OCD threshold

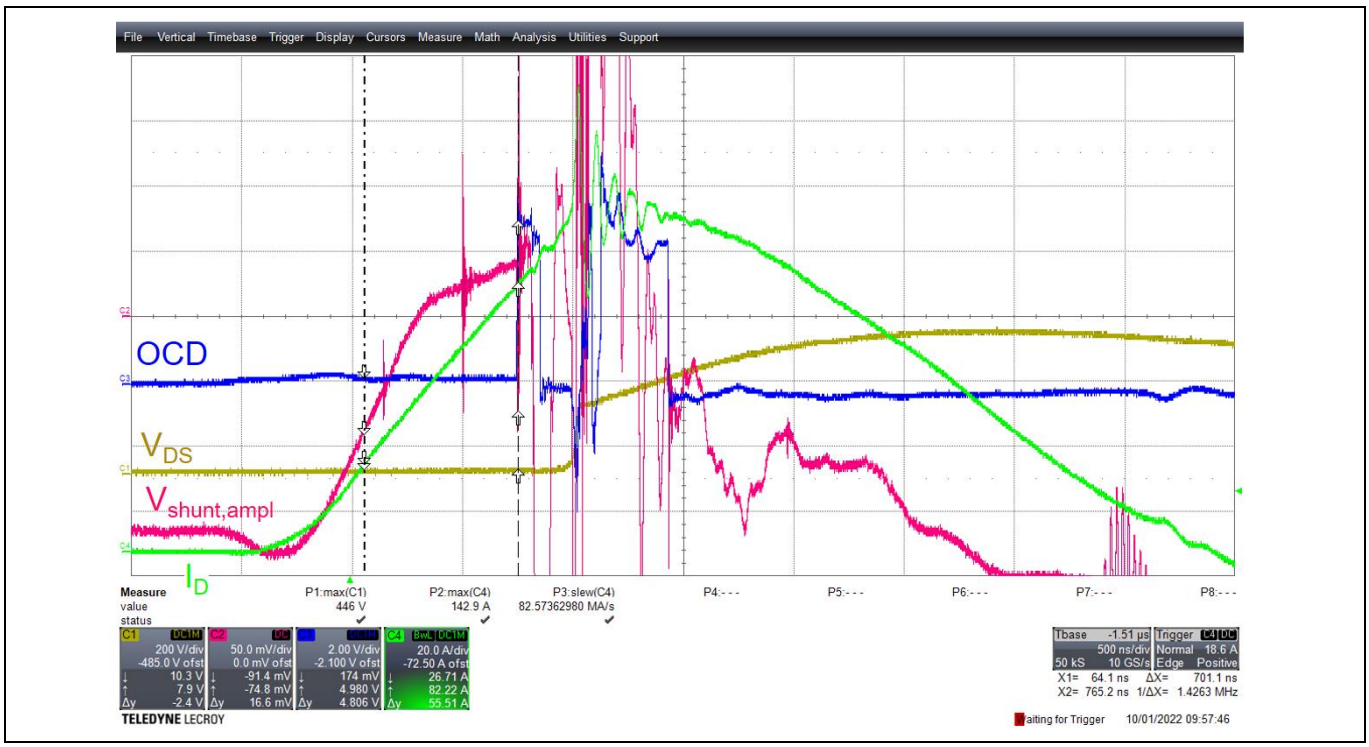

Figure 35 Typical load short circuit turn-off with shunt-based OCD

V_{DS} based OCD:

An OCD for bipolar devices (IGBT) is usually done with DESAT detection. In this case the V_{CE} voltage is measured and if it exceeds a certain threshold voltage, the OCD will be triggered. A similar concept is used for the V_{DS}-based OCD in the eFuse PoC. The drawback of using this concept for a MOSFET device is the $R_{DS(on)}$ change over temperature in the power devices which would result in lowering the overcurrent threshold with higher temperatures. The typical $R_{DS(on)}$ change over temperature for the CoolMOS™ S7A MOSFETs is shown in **Figure 36**. To compensate for this effect, the eFuse PoC uses the on-die temperature sensors and dynamically adjusts the OCD threshold accordingly. In this case a constant and accurate overcurrent threshold over temperature is achieved. The comparison between the overcurrent shutdown with and without compensation is shown in **Figure 37**.

The benefits of using the V_{DS}-based shutdown are lower parasitic inductance and higher $R_{DS(ON)}$ compared to the shunt resistance value giving a higher R/L ratio, resulting in a higher signal output and higher corner frequency in the amplitude response. The V_{DS}-based OCD threshold for different current slew rates is shown in **Figure 38**.

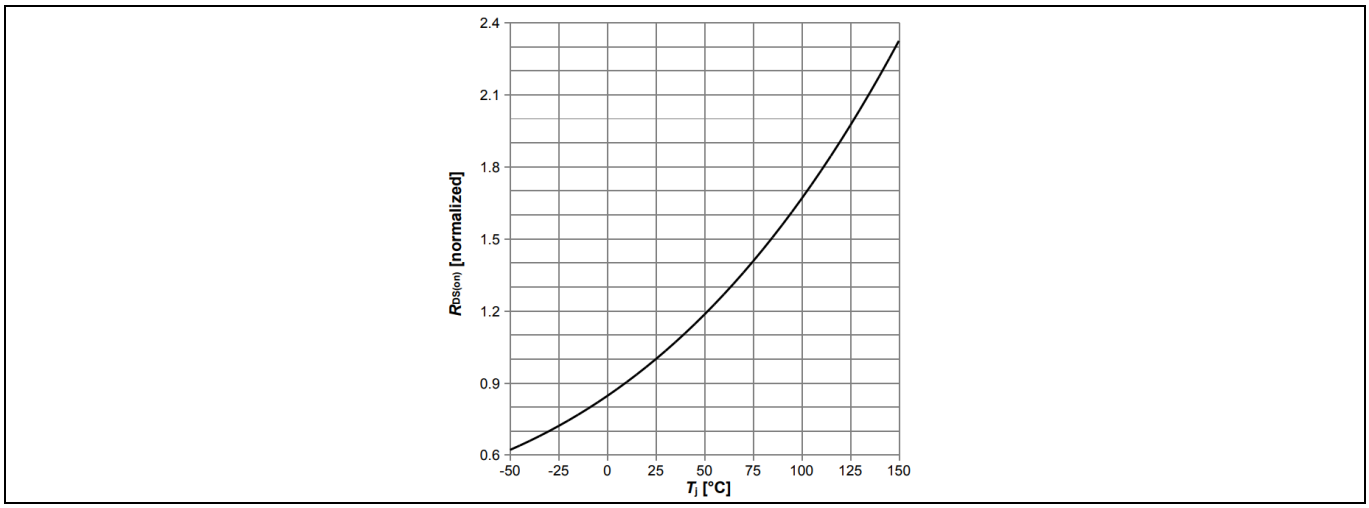

Figure 36 Typical $R_{DS(on)}$ drift over temperature for S7A device [4]

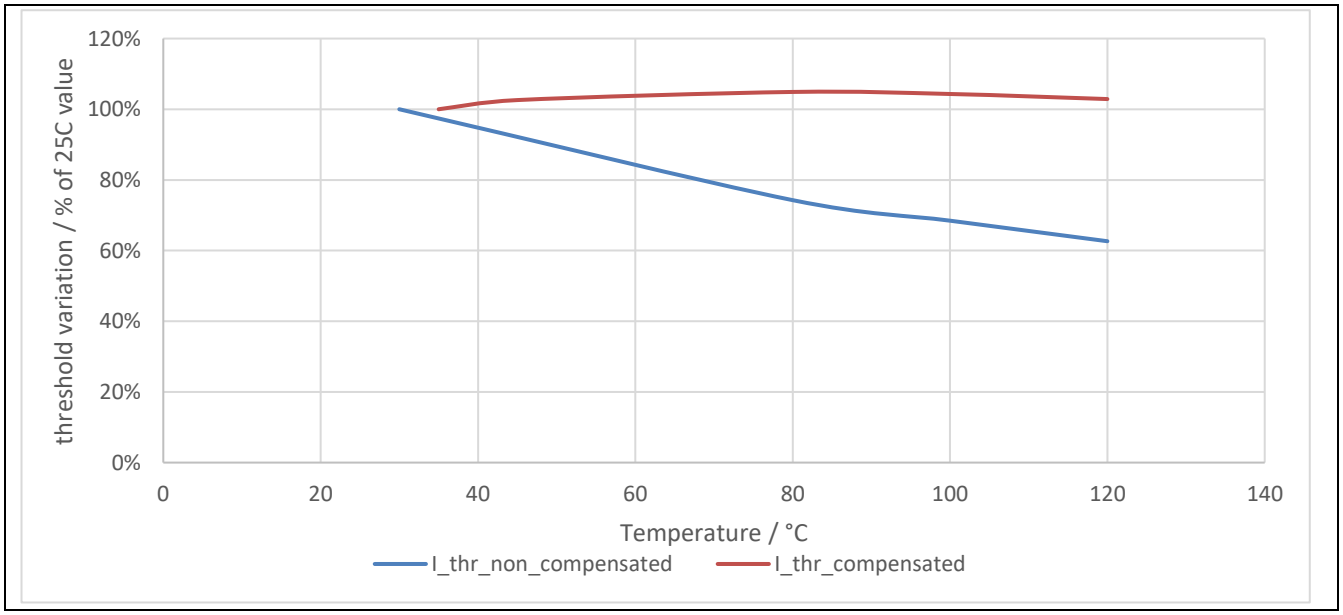

Figure 37 V_{DS} based OCD shutdown with and without temperature compensation

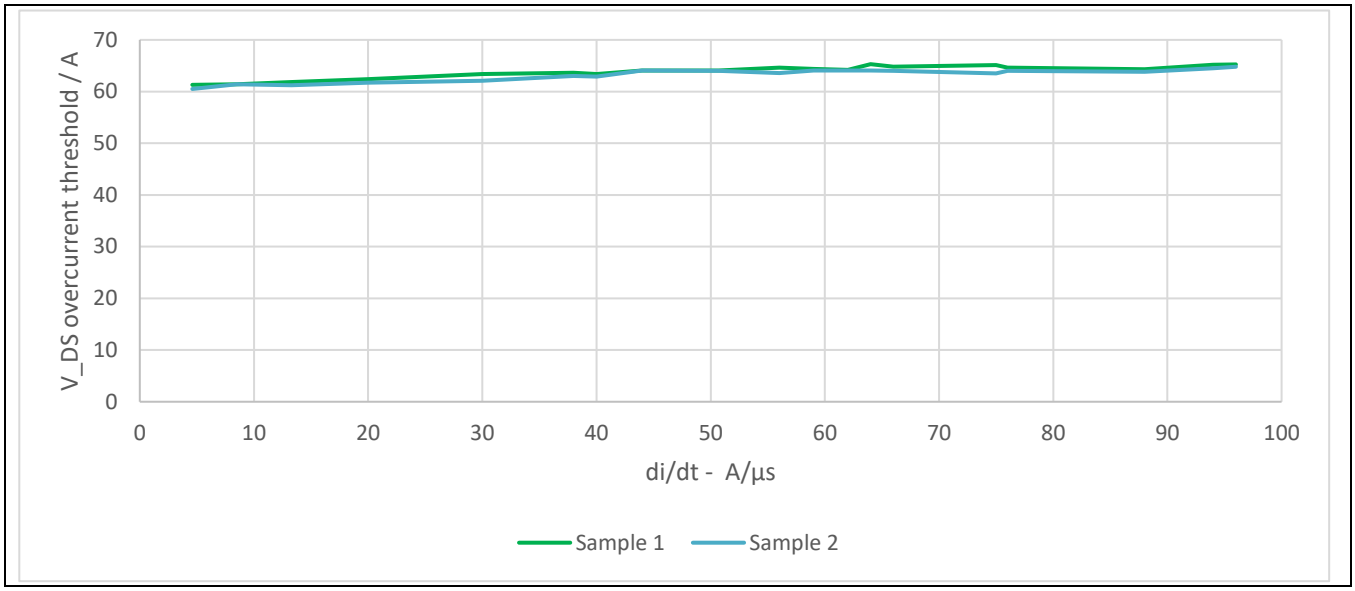

Figure 38 Measurement of V_{DS} threshold variation for different current slew-rates

2.3 Fast turn-off – power device clamping

As discussed in the previous chapters the auxiliary load could include an inductive share while the wiring harness incorporates parasitic inductances. In case of overcurrent events, the eFuse will turn-off the output and the current flow abruptly and therefore the energy stored in those inductances must be dissipated by the eFuse.

When considering the equivalent circuit diagram of the two eFuse short circuit conditions shown in **Figure 28** and **Figure 29**, a potential freewheeling path to the positive terminal of the battery would be possible. This way part of the energy stored in the wiring harness of the system can be freewheeled in case of a short circuit shutdown. As discussed in **Chapter 2.2.2**, the short circuit current will be mainly driven by the bulk capacitors of the connected inverters and the current share from the HV battery is significantly smaller.

If no freewheeling path is available or possible in the application, the power devices cannot handle the power and energy dissipation internally to stay in the safe operating area (SOA) of the device and therefore an external clamping circuit is needed. This clamping could be realized in various ways by applying a transient voltage suppressor (TVS), metal oxide varistor (MOV), or an RC snubber circuit.

The eFuse PoC uses a RC snubber circuit and an optional freewheeling path to protect the power devices during a shut-down, as shown in **Figure 39**. The RC snubber must be dimensioned such that $V_{DS(max)}$ is less than $V_{(BR)DSS}$ during the switch off. **Figure 40** shows the measurement of an overcurrent switch-off event during a load short circuit. The OCD threshold level was set to 65 A and after a delay of ~300 ns the MOSFETs start to turn off, thus the V_{DS} voltage rises. After this, the current through the eFuse is still increasing as the snubber capacitor has to be charged. In approximately 5 µs all the energy of the wiring harness is dissipated, no more current is flowing and the V_{DS} voltage will settle to the battery voltage V_{bat}.

Two main parameters must be considered for the snubber design. The first parameter is the initial voltage step $V_{DS(init)}$ after the power device is turned off. This voltage step can be adjusted with the series resistance of the RC snubber. The second parameter, the overshoot, can be damped with the capacitance to stay below the breakdown voltage $V_{(BR)DSS}$ of the power device. As discussed in **Chapter 2.2.2**, the highest amount of energy to be dissipated by the eFuse occurs during the turn-off of a load short circuit with 42.98 mJ. For clamping this energy, the capacitance value for a defined voltage rise can be calculated as follows:

Implementation

$$C_{snubber} = \frac{2 \cdot E_{clamp}}{V_{DS(\max)}^{\ 2}} = \frac{2 \cdot 42.98\ mJ}{450^2\ V^2} = 424.49\ nF$$

The resistance can be dimensioned for a defined initial voltage step for the worst-case shutdown current in a terminal short circuit condition:

$$R_{snubber} = \frac{V_{DS(\text{init})}}{I_{shutdown}} = \frac{400\ V}{120\ A} = 3.33\ \Omega$$

When dimensioning the resistors in the snubber circuit, the maximum peak power dissipation during this first step must be considered. In the eFuse PoC, anti-surge thick film resistors are used which can withstand a maximum peak power of 4 kW, resulting in a maximum peak power of 24 kW for all resistors.

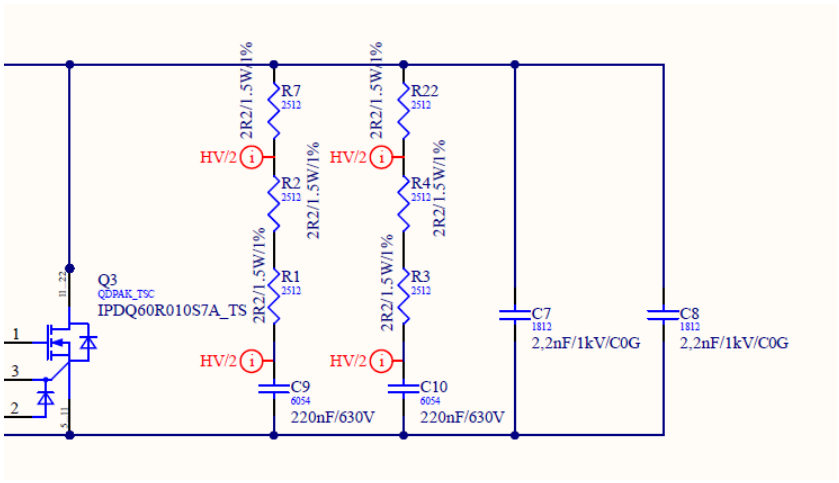

Figure 39 RC snubber design for the eFuse PoC

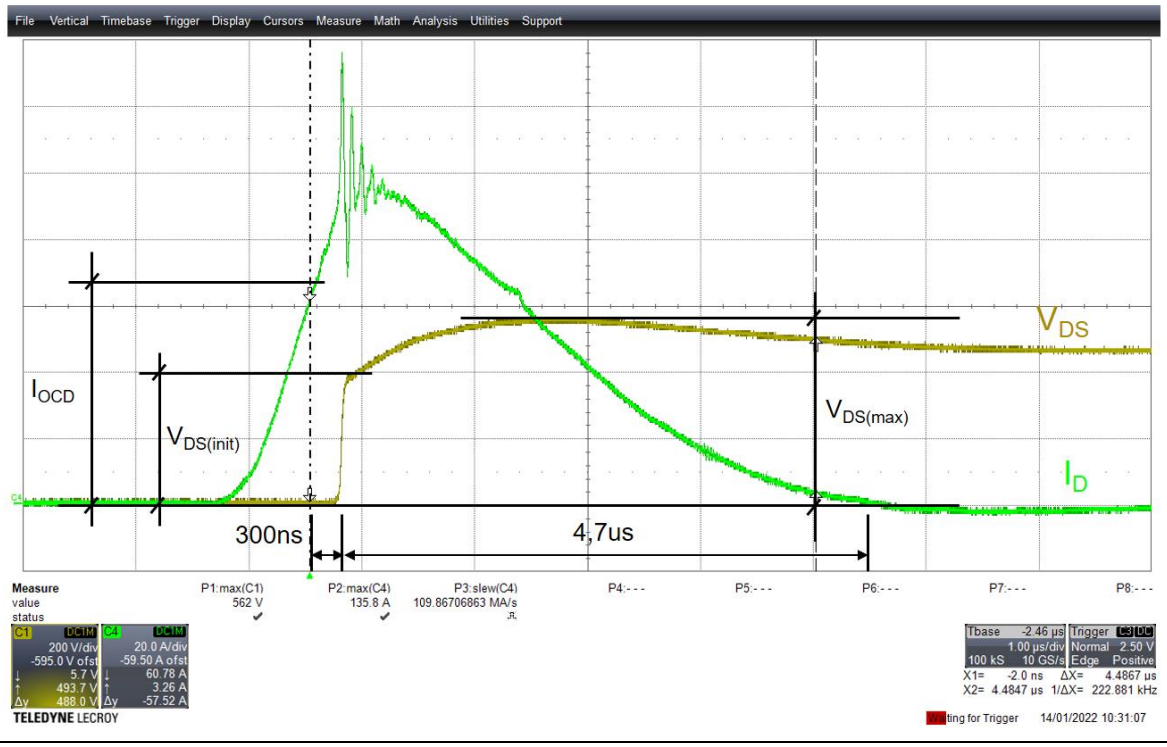

Figure 40 Turn-off of eFuse during load short circuit

2.4 Fast turn-off – freewheeling diode

In order to reduce the energy that needs to be dissipated in the snubber clamping circuit during short circuit turn-offs, a freewheeling diode could be used. In this case, part of the energy can be fed back to the battery instead of being dissipated in the RC snubber circuitry. To assess the benefits and drawbacks, the failure cases must be evaluated on system level as shown in **Figure 41**. The considerations in **Chapter 2.4** covering the switch-off phase of the eFuse with an additional freewheeling path. The conclusions of **Chapter 2.2.2** are cover the initial phase of a short circuit and therefore the slew rates and switch-off currents stay the same.

Load short circuit:
In the case of load short circuit, the energy stored in the wiring harness of the auxiliary load can be dissipated to the battery, but the energy from the battery and the main inverter must be still dissipated in the eFuse snubber circuitry. This would result in a switch-off parasitic inductance of 1.9 µH from the equivalent circuit diagram and the reduced clamping energy can be calculated as follows:

$$E_{LSC,freewheel} = \frac{1}{2} L_{total} \cdot I_{shudown}^2 = \frac{1}{2} 1{,}9\ \mu H \cdot 148.46^2 A^2 = 20.94\ mJ$$

Terminal short circuit:
When using a freewheeling diode in the case of a terminal short circuit case, the complete eFuse system must be considered. In this case part of the energy can still be freewheeled to the battery, but a negative voltage clamping circuit is needed in the auxiliary inverter, as during switch-off, circulation currents through the short circuit and the body diodes of the inverter stage will occur. In this case the eFuse only needs to dissipate the energy of the wiring to the main inverter and the battery. In the short circuit the current share of the main inverter is approximately two-thirds of the overall shutdown current, and the reduced clamping energy can be calculated as follows:

$$E_{TSC,freewheel} = \frac{1}{2} L_{total} \cdot I_{shutdown}^2 = \frac{1}{2} 1.9\ \mu H \cdot 134.47^2 A^2 = 17.18\ mJ$$

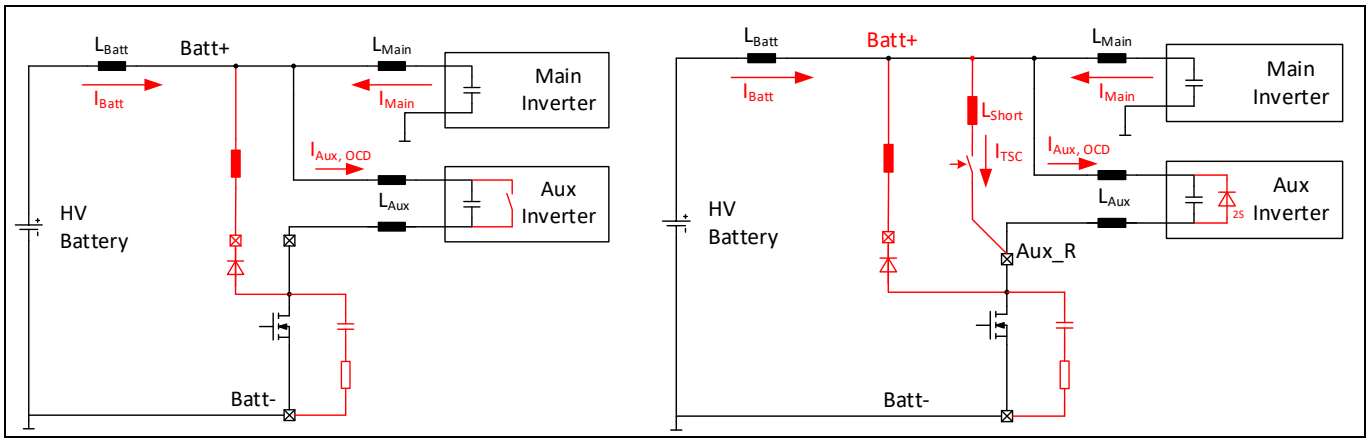

Figure 41 Using a freewheeling diode in load short circuit and terminal short circuit

With the freewheeling diode, the required clamping energies can be reduced for the terminal and load-short circuit in the eFuse application. However, due to compensation processes in the HV boardnet which could for example lead to negative currents in the eFuse, the freewheeling diode could be energized and therefore may not be an option in all boardnet topologies.

The implemented eFuse PoC RC snubber circuitry is dimensioned to cover the short circuit requirements discussed without any additional freewheeling diode.

3 eFuse - PoC hardware implementation

3.1 Key facts

The key goal of the eFuse PoC is to allow application-level evaluation of the CoolMOS™ S7A and CoolSiC™ power devices in combination with a protection and diagnostic concept supporting safety relevant applications.

The key electrical parameters are listed in **Table 14**. In addition to that, the PoC features:

- Second generation safety and protection concept:
  - Redundant and diverse OCD
  - Cooling system diagnostics
  - Die temperature monitoring
  - SOH diagnostics for power stage
- Application-specific clamping:
  - Combination of freewheeling and RC snubber to minimize clamping effort
- CoolMOS™ and CoolSiC™ technology options
- Scalable assembly technology:
  - TSC and heatspreader power stage
  - BSC with standard and advanced PCB technology
- Safe isolated interface and power supply
- Programmability with graphical user interface (GUI):
  - OCD thresholds
  - Overtemperature-warning (OTW) and shutdown (OTS) thresholds
  - SOH levels
  - Test of OCP
  - Readout and export of analog measurements

Table 14 eFuse PoC key parameters

Parameter	Value	Comment
System voltage class	400 V	
Current capability (continuous)	42 A	T_a= 80°C
Current capability	63 A	for 10 s
Additional ripple current	More than 26 A	

3.2 Hardware concept

The eFuse PoC hardware partitioning is shown in **Figure 42**. It consists of three different boards: the safety extra low voltage (SELV) interface board, the discrete driver board and the power stage PCB. In the SELV interface board the safety isolation between the HV discrete driver implementation and the communication interface is implemented. The complete eFuse PoC can be powered and controlled by a single USB interface. The SELV MCU controls all functions of the discrete driver implementation via an isolated serial peripheral interface (SPI) and supplies the driver PCB with an isolated DC-DC converter as shown in **Figure 43**.

If a USB connection is not available or wanted, the PoC supports the direct control and supply with the connector P1. Additional low-current outputs (open-drain with pull-up resistors) are located at connector P8 and can be used to control e.g., an external short-circuit switch, for example. In addition to that, P5 supports two high-current low-side switches with freewheeling diodes to control relays (e.g., to control a battery main switch).

The discrete driver board uses a microcontroller to operate all hardware related functions and protection features. Furthermore, the current measurement and OCP is implemented, as well as the temperature readout and SOH diagnostic functionality. Depending on the output stage technology, the gate driver voltage can be selected between low voltage (13 V for CoolMOS™ technology) and high voltage (18 V for CoolSiC™ FETs).

The power PCB is exchangeable and connected to the driver PCB with a signal and power connector. Besides the power devices and the shunt resistor, it incorporates the RC snubber circuit, additional on-board temperature sensors and the shunt signal conditioning. Additional buffers for the analog shunt signal are provisioned to ensure signal integrity despite the exchangeable power PCB.

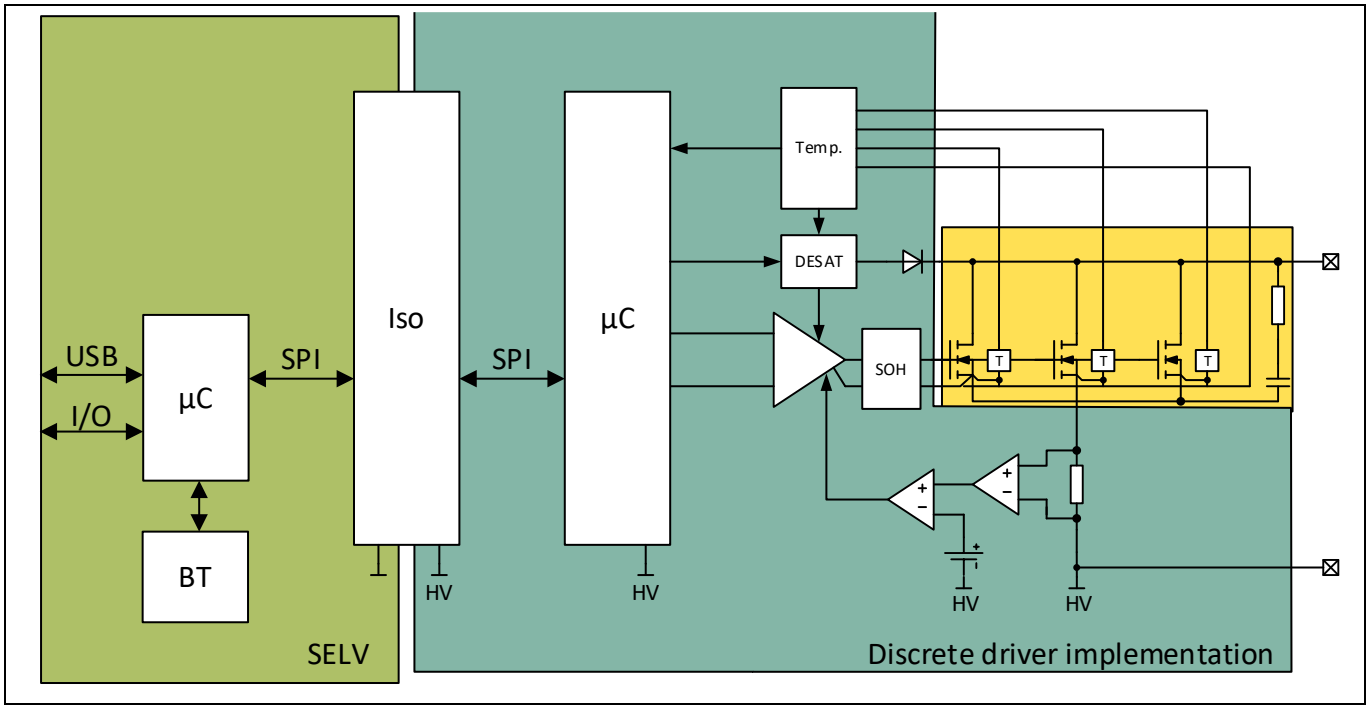

Figure 42 eFuse PoC hardware partitioning

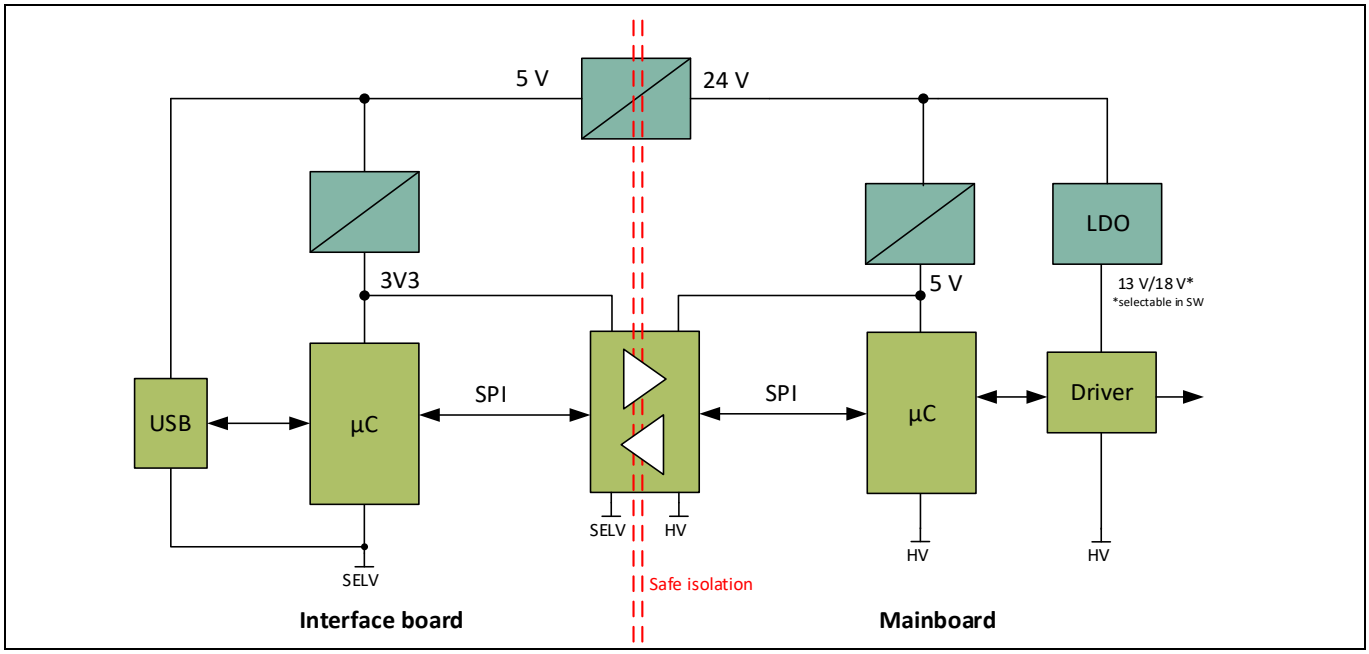

Figure 43 eFuse PoC supply and isolation concept

3.3 Hardware overview

The full eFuse PoC demonstrator setup with a TSC power stage without any heatsink is shown in **Figure 44**. The load and the battery can be connected with the power connector P2 on the driver PCB. The digital SELV interface and supply of the demonstrator are connected with a Micro-USB cable on P3.

A status LED on each MCU board blinks when the MCU is ready and functional. In addition, the driver board has two warning LEDs: one indicating any error (e.g., OCD, OTS, off-state) and another to indicate when any high voltage is present on the fuse (in the off-state). These status LEDs and the eFuse PoC without the power stage connected are shown in **Figure 45**.

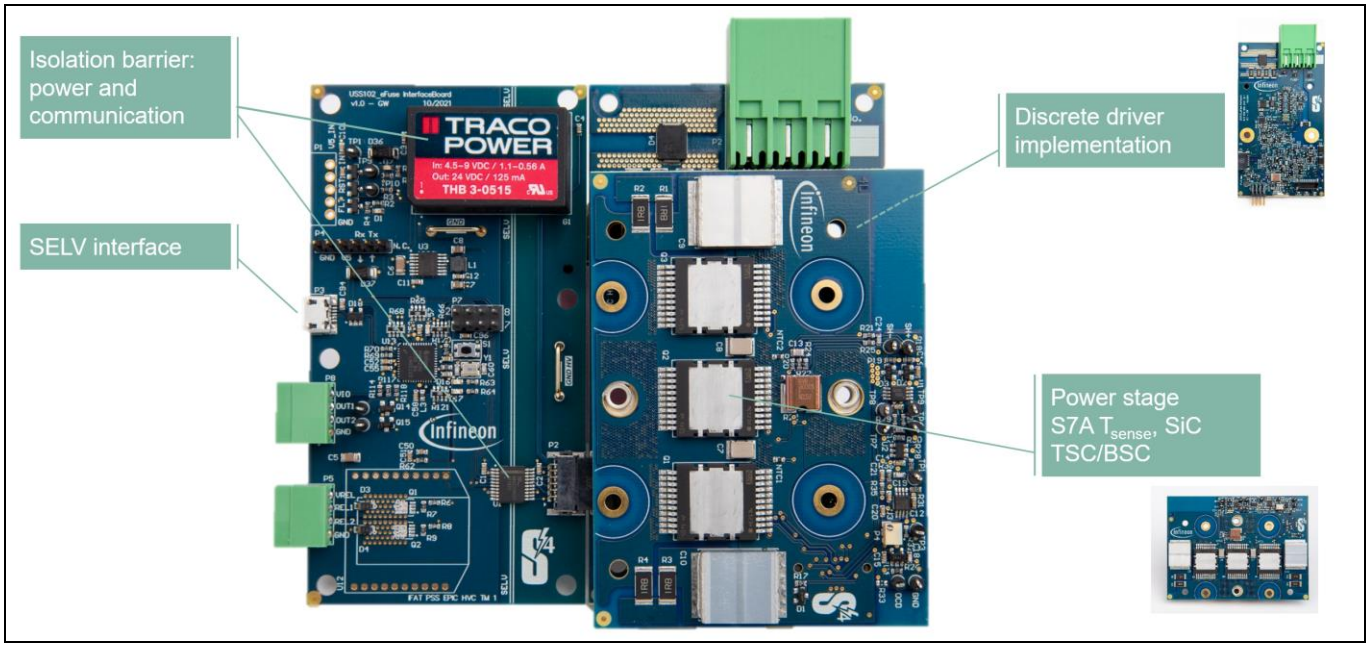

Figure 44 eFuse PoC with TSC power stage connected

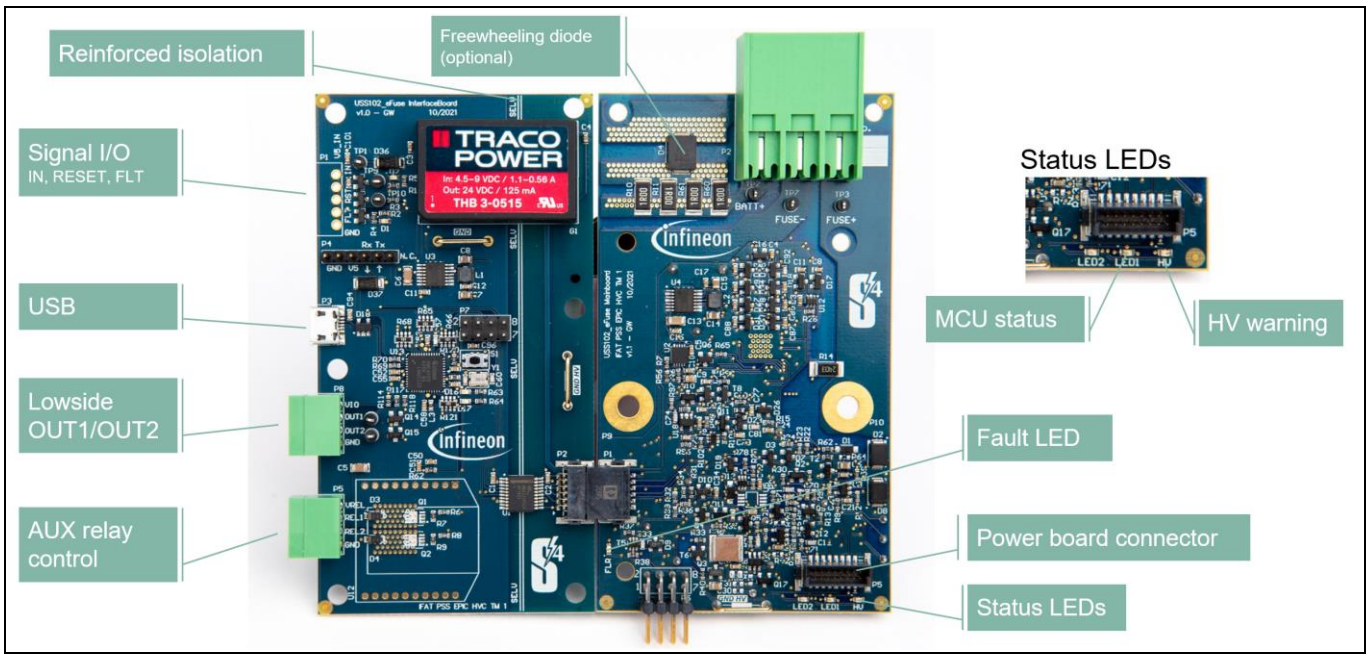

Figure 45 eFuse PoC without power stage

3.3.1 Connector description

All connectors and the appropriate matching connector names are listed in **Table 15**.

Table 15 Connectors description

Designator	Description	Manufacturer	Mating part number
P1 (I/F board)	External supply and control/feedback connector	Phoenix Contact	FK-MC 0,5/ 5-ST-2,5
P3 (I/F board)	USB connector	-	USB A/B connector
P8 (I/F board)	External general-purpose output	Phoenix Contact	FK-MC 0,5/ 4-ST-2,5
P5 (I/F board)	External relay control outputs	Phoenix Contact	FK-MC 0,5/ 4-ST-2,5
P2 (I/F board)	SPI and supply connection to mainboard	Phoenix Contact	FP 1,27/ 12-MH
P1 (mainboard)	SPI and supply connection to I/F board	Phoenix Contact	FP 1,27/ 12-FH
P2 (mainboard)	Power connectors for eFuse	Phoenix Contact	LPC 6/ 3-ST-7,62

3.3.2 eFuse BSC measurement results

The eFuse BSC layer stack is implemented as discussed in **Chapter 2.1.4**, including the galvanic isolation in the PCB with a standard extruded heatsink without any active cooling. The implementation shown in **Figure 46**, uses a conductive TIM between the PCB and the heatsink and is screwed together with the power stage. Areas of the PCB which are not on SELV level are milled out of the heatsink. For high-current measurements, the current is directly fed into connectors of the power stage, not using connector P2 on the mainboard.

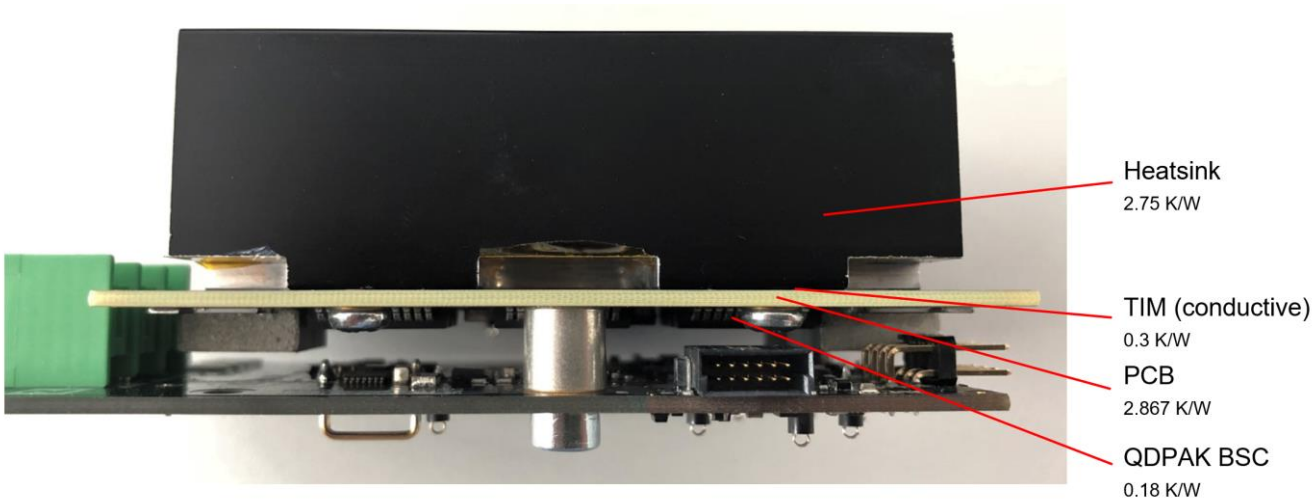

Figure 46 eFuse BSC power stage implementation

The thermal measurements are done considering the load profile discussed in **Chapter 1.4** and are captured using the eFuse PoC. The layout and the location of the board NTCs are shown in **Figure 47**. The PCB uses filled and capped µvias directly underneath the exposed pad, which are then stacked with buried vias to connect to the third layer. To ensure safe isolation of the heatsink, two layers of PrePreg are used to isolate the interface layer from the heatsink.

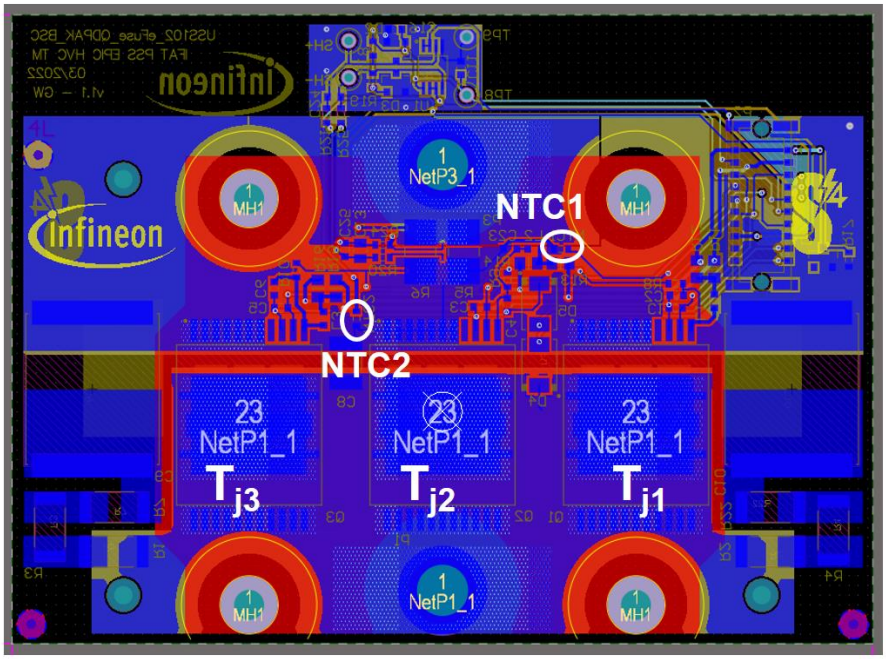

Figure 47 eFuse BSC power stage layout

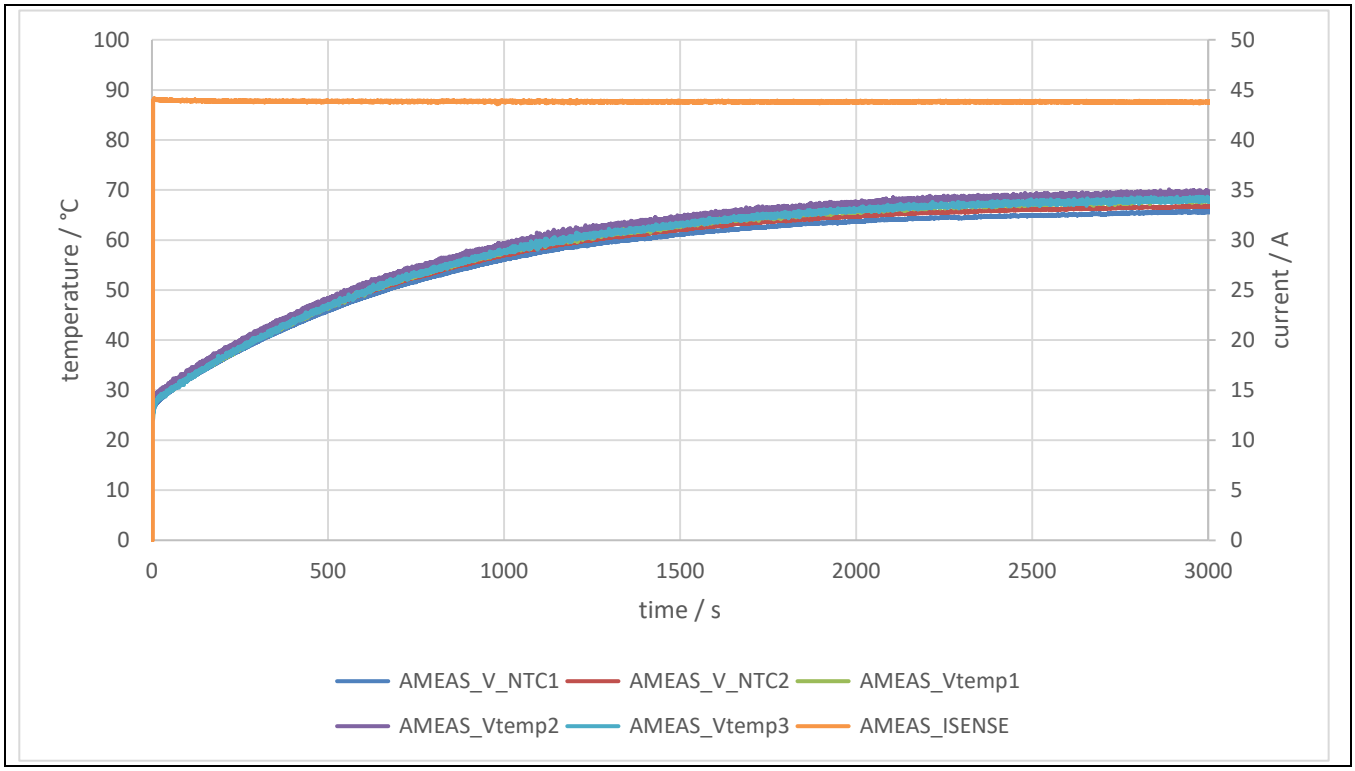

Figure 48 eFuse PoC BSC power stage – 42 A DC measurement result

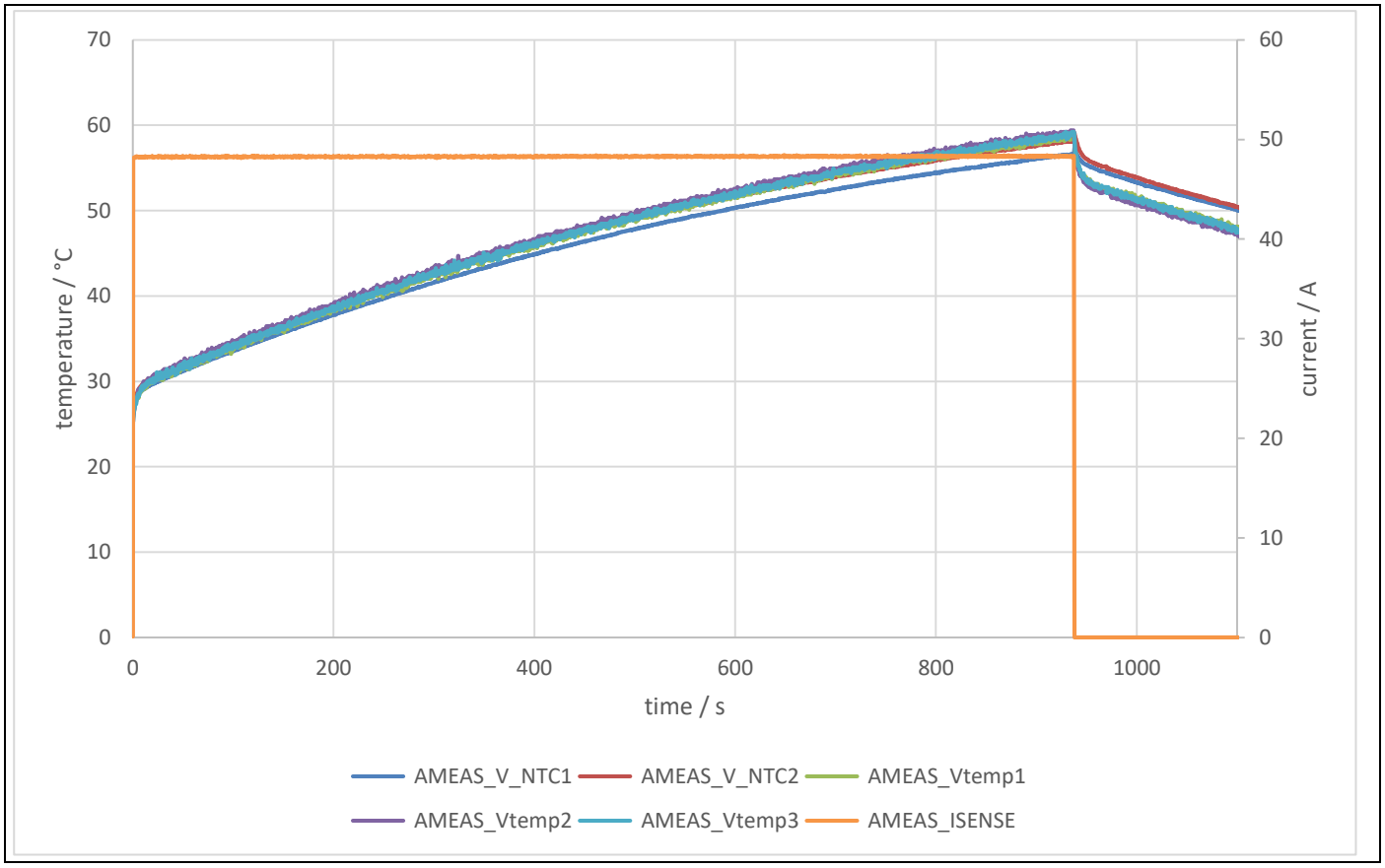

Figure 49 eFuse PoC BSC power stage – 46 A – 900 s measurement result

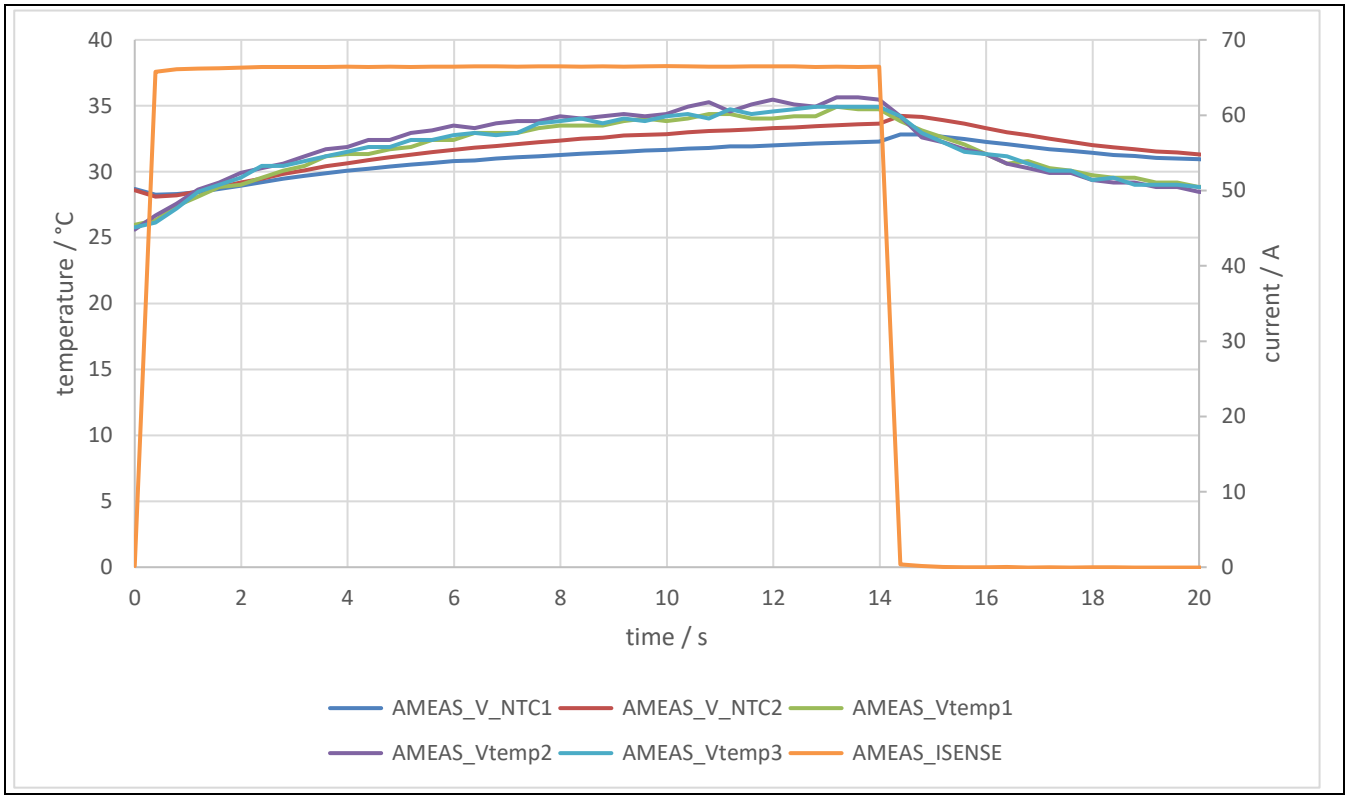

Figure 50 eFuse PoC BSC power stage – 63 A – 10 s measurement result

In the measurement results shown in **Figure 48**, **Figure 49** and **Figure 50** it can be seen that the NTCs are still following the embedded temperature sensors because of the low heating slew rate. If the current and the heating slew rate increase, the external sensors cannot detect them anymore, which is shown in **Figure 51**. In this case the discrete sensors show already a difference of ~10°C and this error will increase for higher currents.

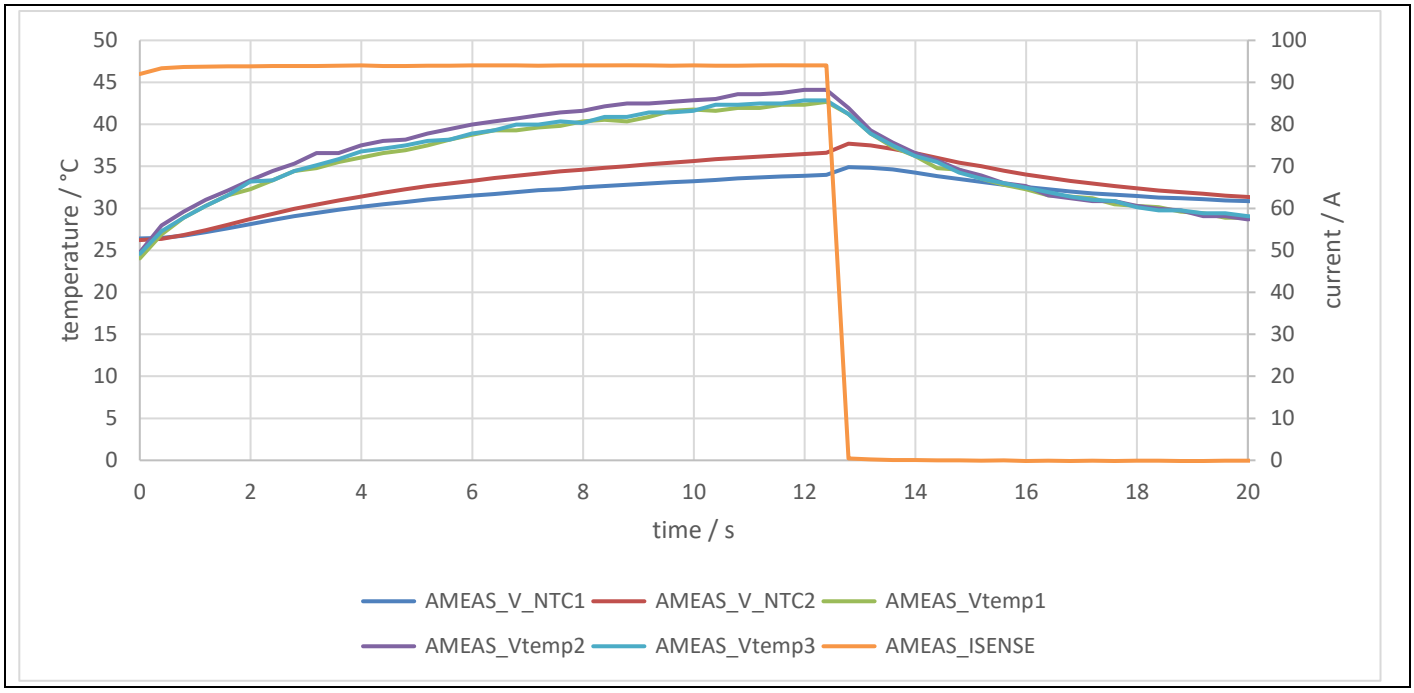

Figure 51 eFuse PoC BSC power stage – 89 A measurement result

3.3.3 eFuse TSC measurement results

To achieve the best cooling performance, the TSC version of the QDPAK package is used in the eFuse PoC as discussed in **Chapter 2.1.1**. This implementation uses heatspreaders that are directly soldered onto the devices to increase the thermal capacitance and contact area to the heatsink as shown in **Figure 52**. An additional isolation layer is needed towards the heatsink and this is achieved with a Kapton tape. The layout and position of the external NTCs and junction temperature sensors is shown in **Figure 53**.

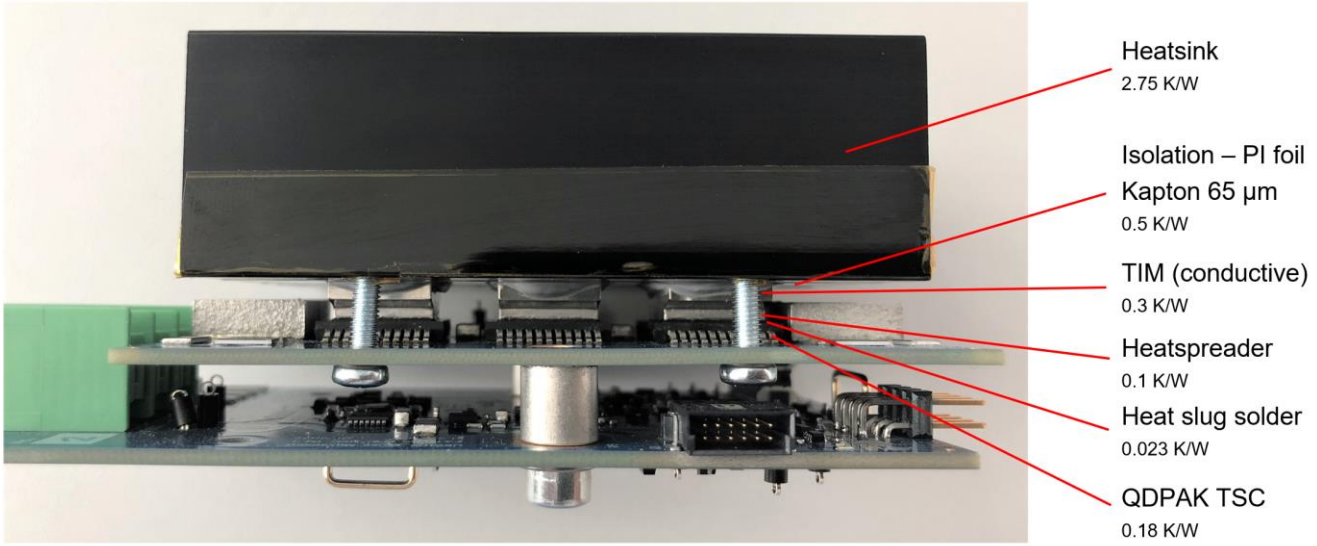

Figure 52 eFuse TSC power stage implementation

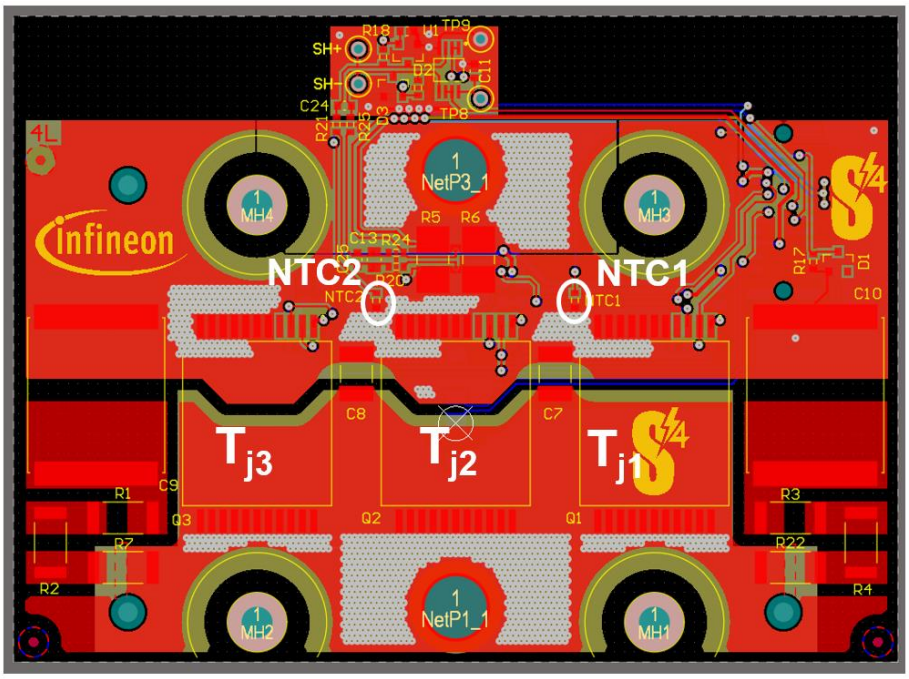

Figure 53 eFuse TSC power stage layout

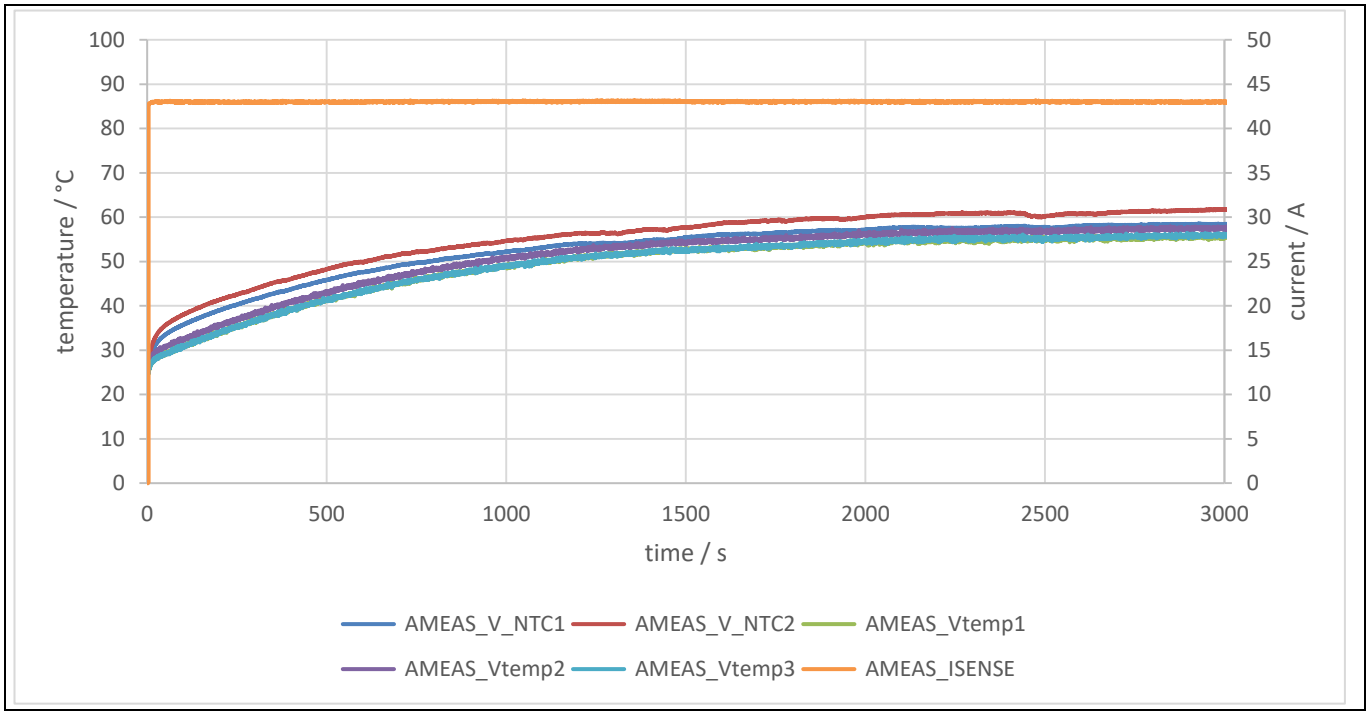

Figure 54 eFuse PoC TSC power stage – 42 A DC measurement result

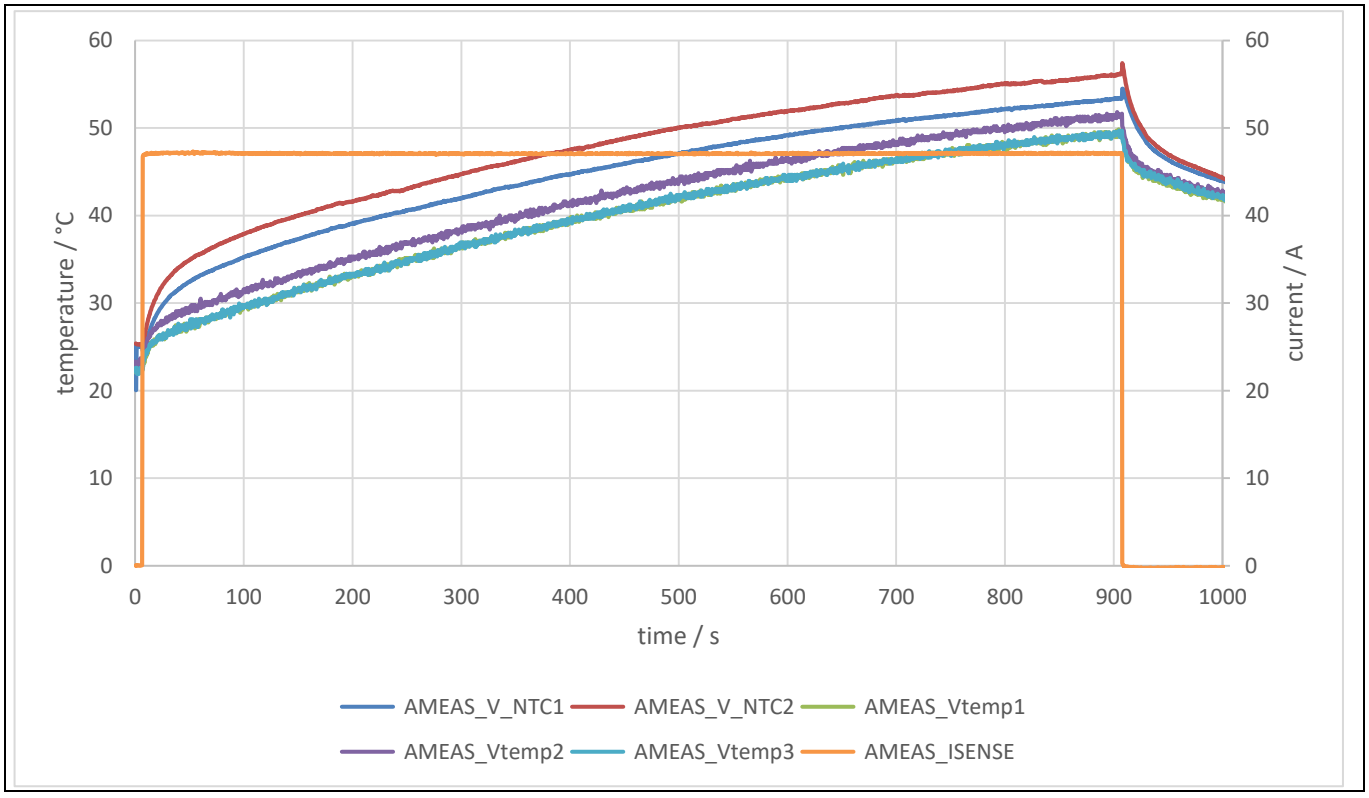

Figure 55 eFuse PoC TSC power stage – 46 A – 900 s measurement result

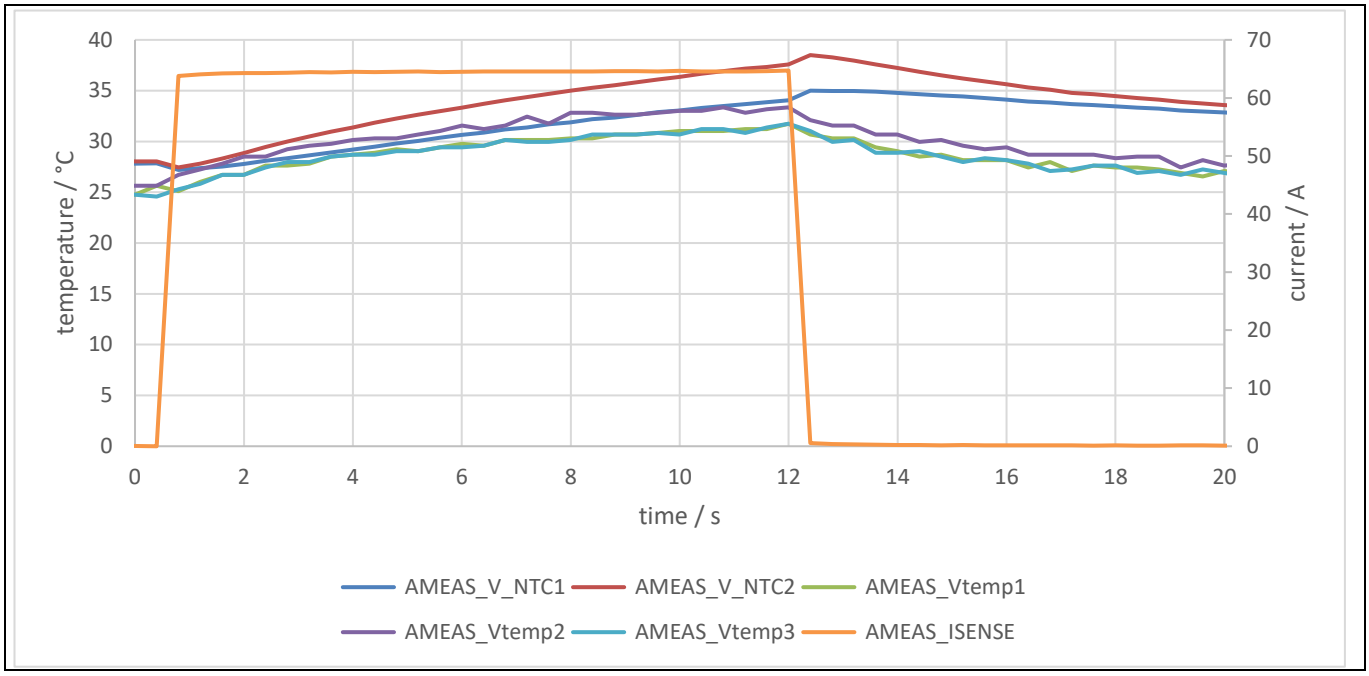

Figure 56 eFuse PoC TSC power stage – 63 A – 10 s measurement result

3.3.4 eFuse TSC vs. BSC results comparison

For comparison reasons the junction and NTC temperature measurements are averaged for the TSC and BSC. **Figure 57**, **Figure 58** and **Figure 59** shows the difference between the TSC and BSC solution for different load patterns. The TSC variant gives an advantage of ~12°C in the nominal eFuse current in the steady state. As the BSC version also includes cooling for the PCB, the NTC temperatures show a lower temperature than the junction temperatures. For the TSC implementation the effect is different and the discrete PCB sensors show higher junction temperatures, especially for higher current pulses.

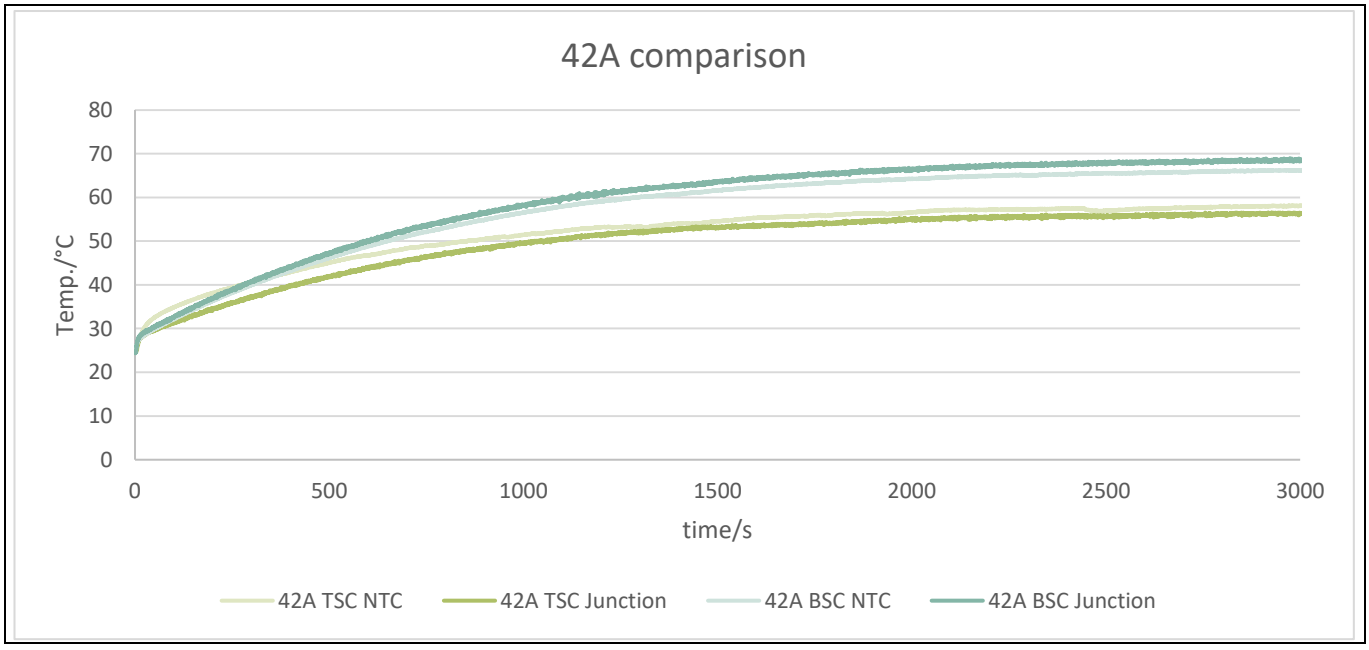

Figure 57 eFuse PoC – 42 A DC measurement comparison-TSC vs. BSC

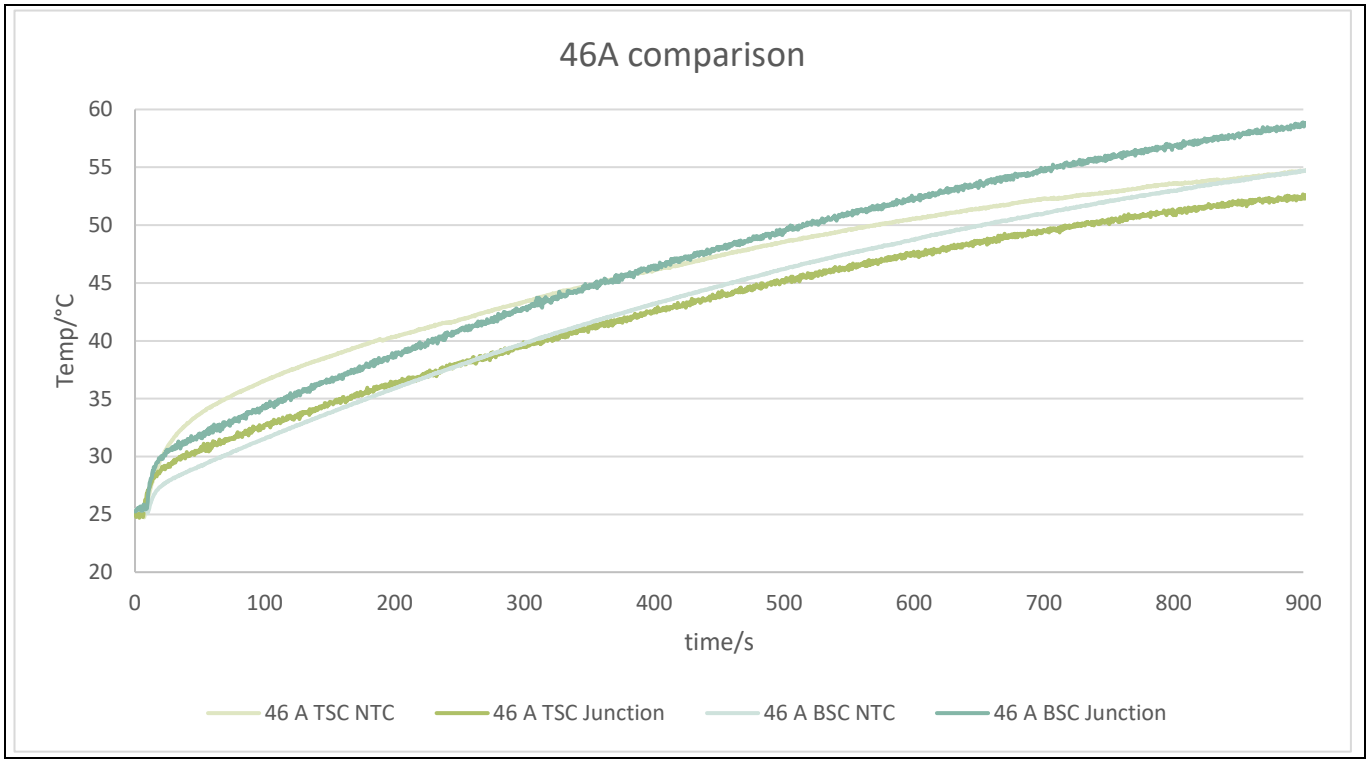

Figure 58 eFuse PoC – 46 A – 900 s measurement comparison – TSC vs. BSC

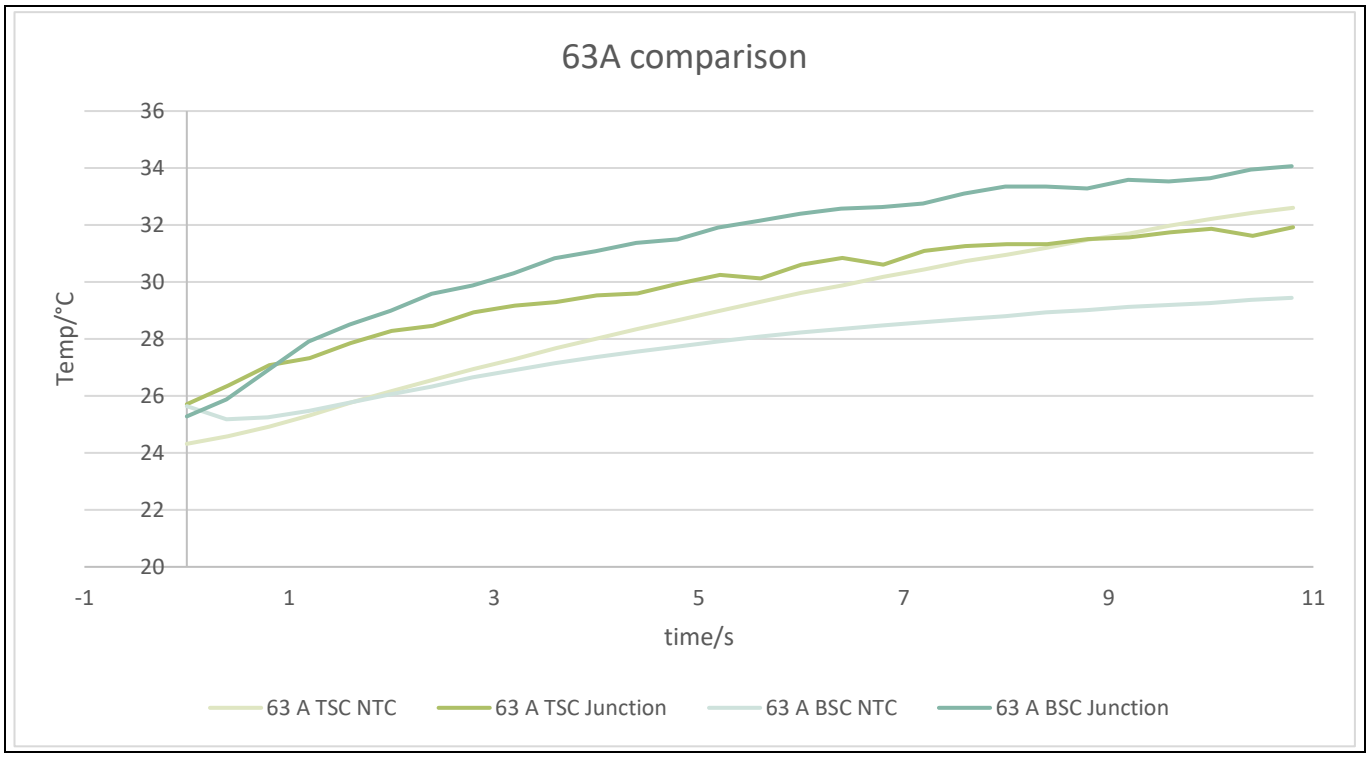

Figure 59 eFuse PoC – 63 A – 10 s measurement comparison - TSC vs. BSC

3.4 eFuse PoC GUI

The easiest method to control the eFuse PoC is by using the Windows GUI software and the USB interface. After connecting the demonstrator for the first time, the Infineon WinUSB driver must be installed. After successful installation of the driver, the eFuse PoC is ready for operation.

After starting the software, the main window is shown, as in **Figure 60**. If the device is connected and working properly (both status LEDs blinking) the GUI shows “1 – Infineon WinUSB Device” in the USB Connect window.

Note: The Infineon WinUSB driver must be installed via the device manager in advance. Otherwise, the “Infineon WinUSB Device” will not be shown in the Connect window.

When the Infineon WinUSB Device is selected in the drop-down menu, the PoC can be connected by clicking “Connect”. A successful connection will be indicated in the “Status message window”. When connected the periodic readout can be started with the button “Start Readout”. All analog parameters and status flags are now read out periodically and displayed in the GUI.

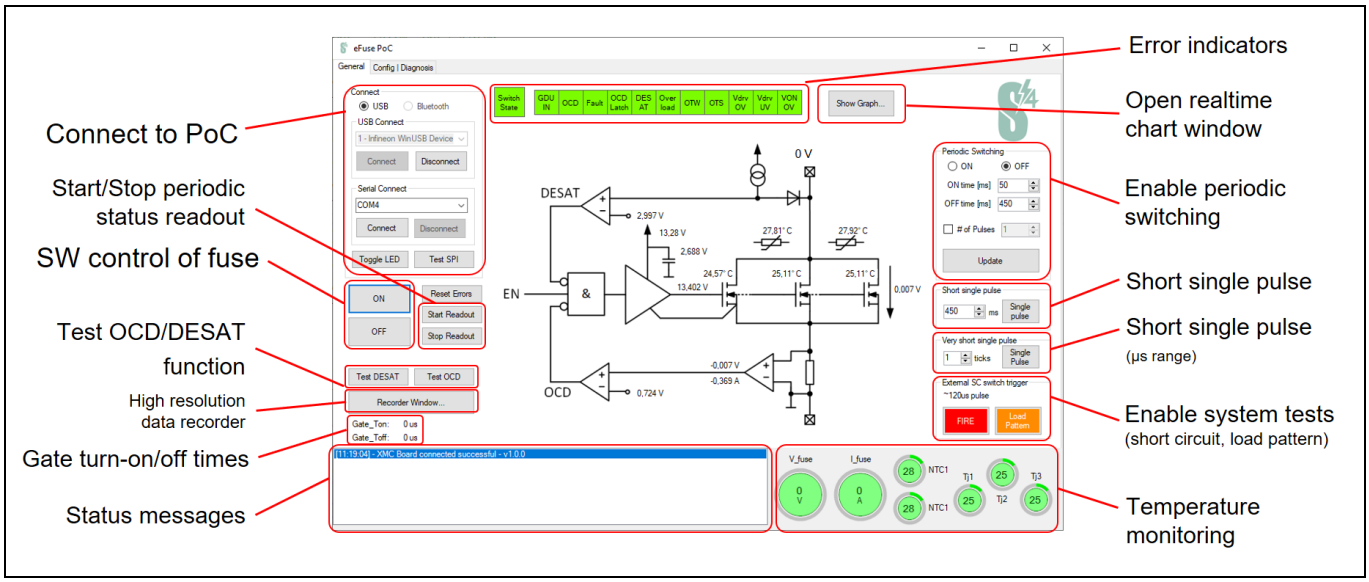

Figure 60 eFuse PoC software main window

Functions that can be activated in the main window are shown in **Table 16** and the status indicators are described in **Table 17**.

Table 16 Functions overview of the main window

Function/Button	Description
Connect/Disconnect	Connect and disconnect the eFuse PoC to the GUI
On/Off	Turn eFuse switch on or off – continuously
Reset errors	Resets any error flags if possible
Start/Stop readout	Starts or stops the periodic status and analog readout
Test OCD/DESAT	Initiates an OCD or DESAT test (test of complete signal path)
Recorder window	Opens the high-resolution recorder window
Gate turn-on/turn-off times	Readback of the gate turn-on and turn-off times when switching the eFuse

Function/Button	Description
Status message window	Indicates any problem with the eFuse communication or functions
Error indicators	Representation of the status flags (see **Table 17**)
Show graph	Shows the real-time graph of all analog measurements
Enable periodic switching	Activates or deactivates the periodic switch for unlimited or a number of pulses with a defined On and Off time
Short single pulse	Activates the eFuse for a single pre-defined short pulse-length (ms range)
Very short single pulse	Activates the eFuse for a very short single pulse (µs range)
External short circuit switch trigger	Used to activate an external short circuit switch on OUT1 and OUT2
Temperature monitoring	Shows the current die and board temperatures as well as the current voltage and current of the eFuse (see **Figure 61** and **Table 17**)

Table 17 Functions of the error/status indicators

Error indicator	Function
Switch state	Current eFuse state – green…closed; red…open
GDU in	MCU output/gate driver input level
OCD	Shunt-based OCD
Fault	Any fault condition
OCD latch	Latched overcurrent status (shunt or V_{DS}-based)
DESAT	V_{DS}-based OCD status
Overload	Analog current measurement overload
OTW	Overtemperature warning (any temp sensor)
OTS	Overtemperature shutdown (any temp sensor)
Vdrv OV	Gate driver supply overvoltage
Vdrv UV	Gate driver supply undervoltage
VON OV	Vfuse overvoltage error (Vfuse has to be more than 10 V for turn-on)

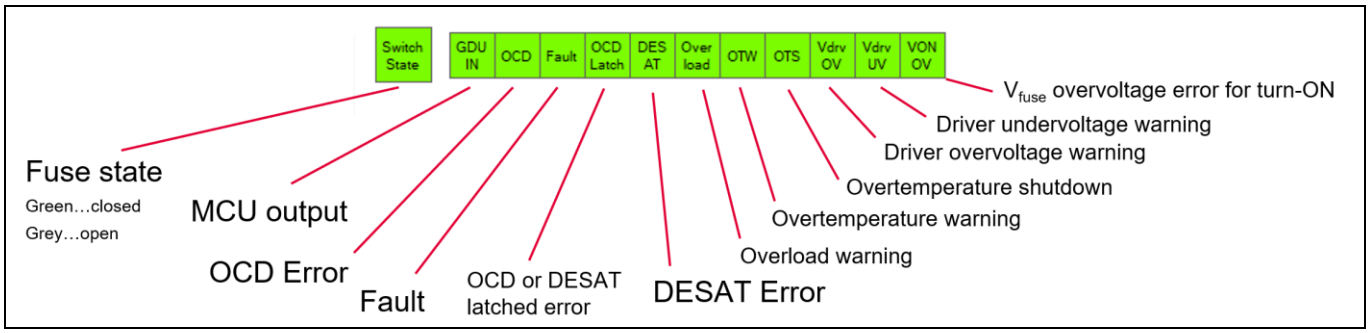

Figure 61 GUI error indicators

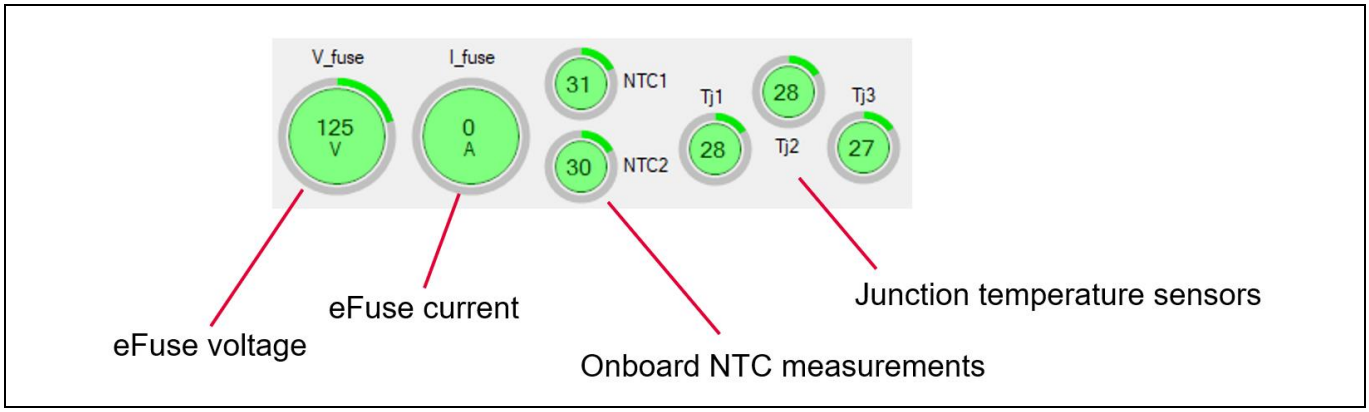

Figure 62 GUI temperature, current, and voltage indicators

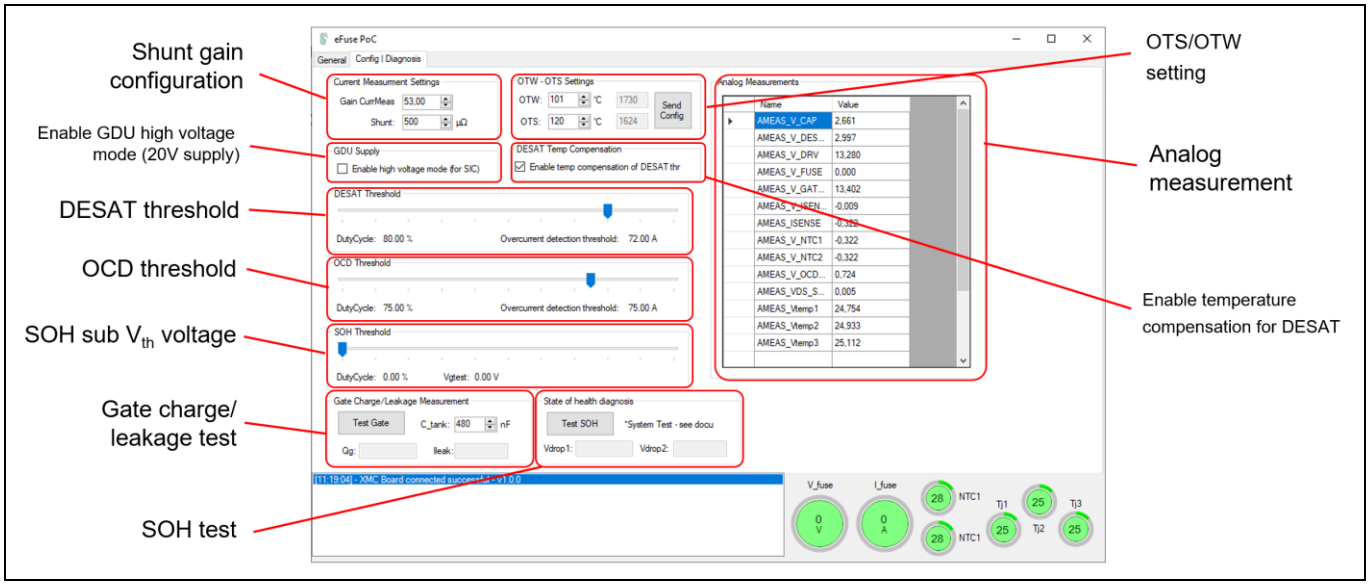

Figure 63 eFuse software configuration window

Figure 63 shows the configuration and diagnosis window.

Attention: When changing the OCD or DESAT thresholds, it is necessary to stay in the SOA of the connected power stage to avoid damage ($V_{DS(max)}$ < $V_{(BR)DSS}$). See Chapter 2.3 for more information.

Table 18 eFuse software configuration window parameters

Function/Button	Description
Shunt/Gain configuration	Configuration for analog current measurement
Enable GDU HV mode	Enable the HV gate driver supply for CoolSiC™ output stage
DESAT threshold	Configuration for the V_{DS} OCD
OCD threshold	Configuration for the shunt base OCD
SOH Vth voltage	Sub-Vth test voltage for state-of-health diagnostics
Gate charge/leakage test	Start the gate charge and gate leakage measurement. VBat should not be supplied during test routine in PoC
SOH test	Start the state-of-health diagnosis; additional BMS switch is required

Function/Button	Description
Analog measurement	Display of all analog measurements in a tabular form
Enable temperature compensation	Enables or disables the temperature compensation for DESAT OCD

3.4.1 eFuse GUI – real-time graph window

When periodic readout is enabled in the main window, all analog measurements can be displayed in the real-time graph with an update rate of ~200 Hz. All data are saved, regardless of whether the channel is activated or not, and can only be cleared by pressing the “Clear Chart” button. **Figure 64** shows the real-time chart window. In addition to the analog signals, all status flags can be displayed as well. By default, all previous data are shown, but there is an option to enable roll mode which only displays data from the last 10 s.

When exporting data to a *.csv file, only the selected channels will be exported.

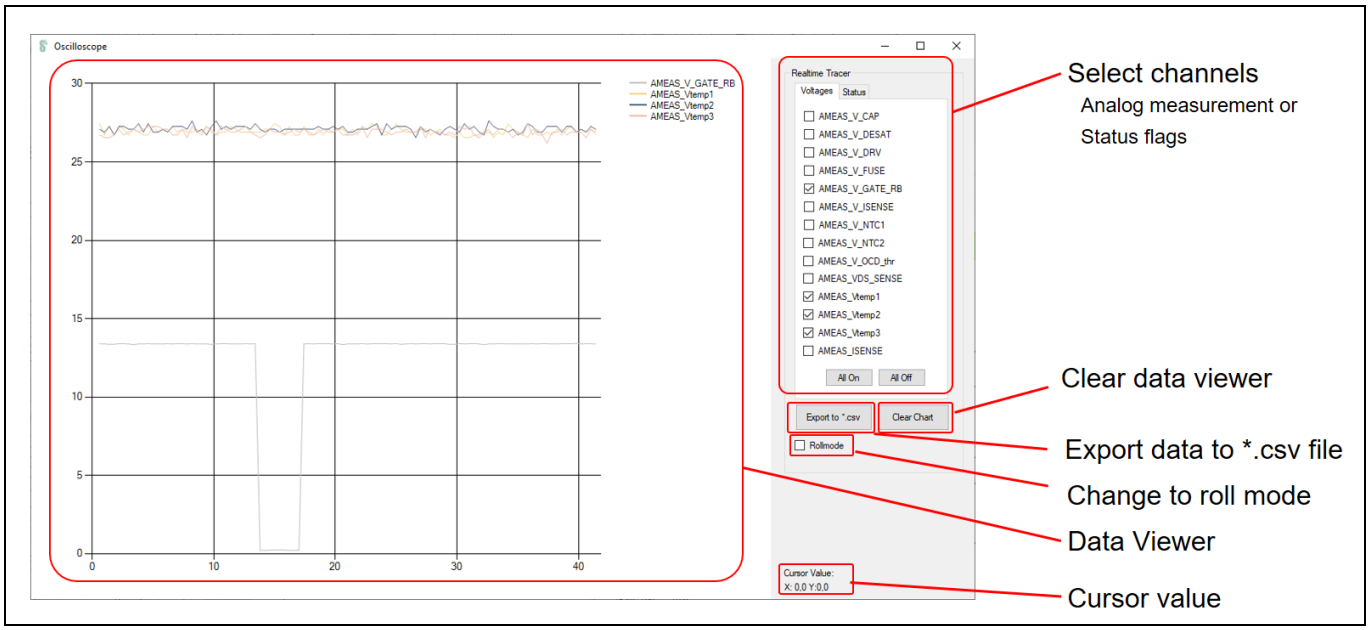

Figure 64 GUI – real-time chart window

3.4.2 eFuse GUI – high-resolution data recorder

The real-time readout of the analog measurements only supports a limited frame rate. If a higher sample rate is needed, the high-resolution data recorder comes into play. With this data recorder, two selected channels will be recorded with a sample rate of ~5 kS and can be triggered by a selected event. The number of recorder samples will be a constant 512 samples, which results in a minimum recording length of 102.4 ms. If longer recording times are needed, the sample rate can be reduced with a pre-scaler. If a hardware trigger is not required, the recording can be started with a manual software trigger in the GUI. The recorder will record 200 samples prior to the trigger event.

Sequence to start a recording:

1. Select recording channel and trigger source
2. With “Recorder Trigger Start” the recorder will be ready and will wait until a trigger event occurs. The status message will be “Waiting…”
3. When the trigger initiates the recording, the status message will change to “Recording…”
4. When the recording finishes, the data will be transferred and displayed in the chart.

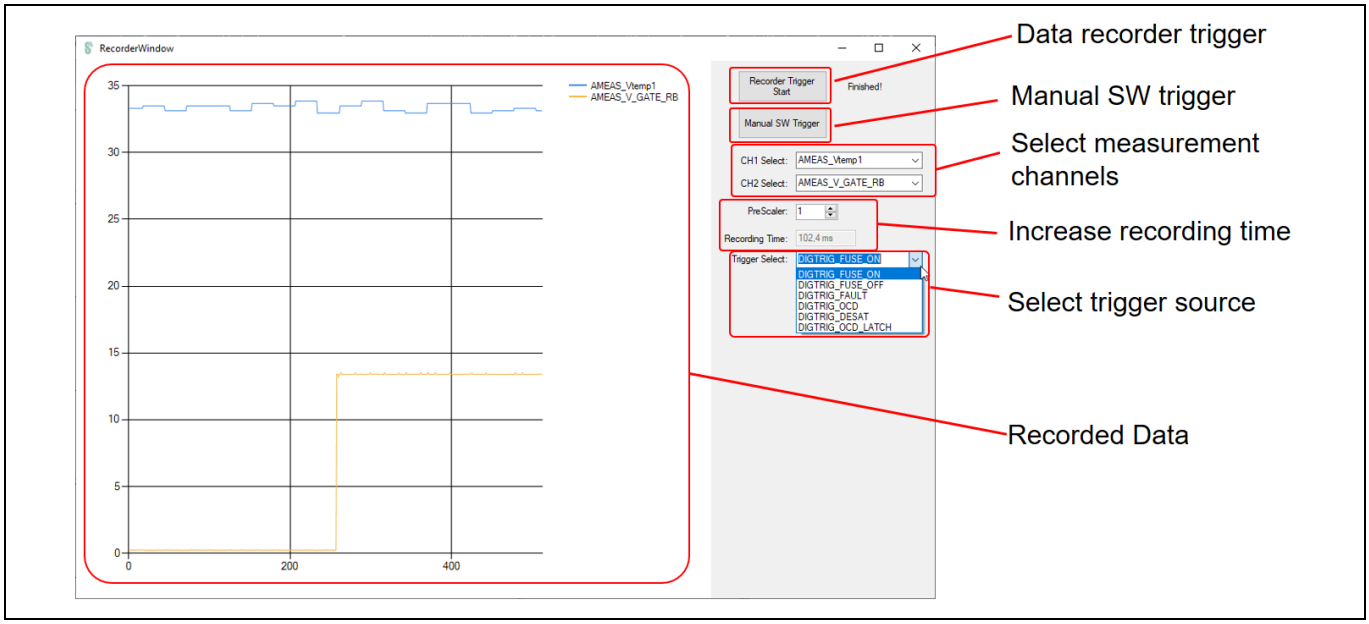

Figure 65 eFuse GUI high resolution recorder window

Table 19 High resolution recorder trigger sources

Trigger source	Description
DIGTRIG_FUSE_ON	Recording starts when the eFuse turns on
DIGTRIG_FUSE_OFF	Recording starts when the eFuse turns on
DIGTRIG_FAULT	Recording starts when a fault condition is detected
DIGTRIG_OCD	Recording starts when the shunt-based OCD is initiated
DIGTRIG_DESAT	Recording starts when the V_{DS}-based OCD is initiated
DIGTRIG_OCD_LATCH	Recording starts when either an OCD or V_{DS} OCD event is initiated

3.5 eFuse PoC quick startup

The basic setup to startup the eFuse PoC in a low-side configuration is shown in **Figure 66**. For power supply and communication of the eFuse PoC a single USB connection is needed. The power supply and the load will be connected to the power connector on the PoC. The steps to get the demonstrator running are as follows:

1. *Connect USB connector to the eFuse PoC – both MCU status LEDs should be blinking.*
2. *Install "Infineon WinUSB" driver in the device panel (only needed for the first time).*
3. *Startup eFuse PoC GUI software.*
4. *Select "Infineon WinUSB Device" in the connect drop-down menu.*
5. *Click "Connect".*
6. *Connection successful message should be displayed in the status message panel.*
7. *eFuse is ready and can be turned on.*
8. *Enable load supply.*

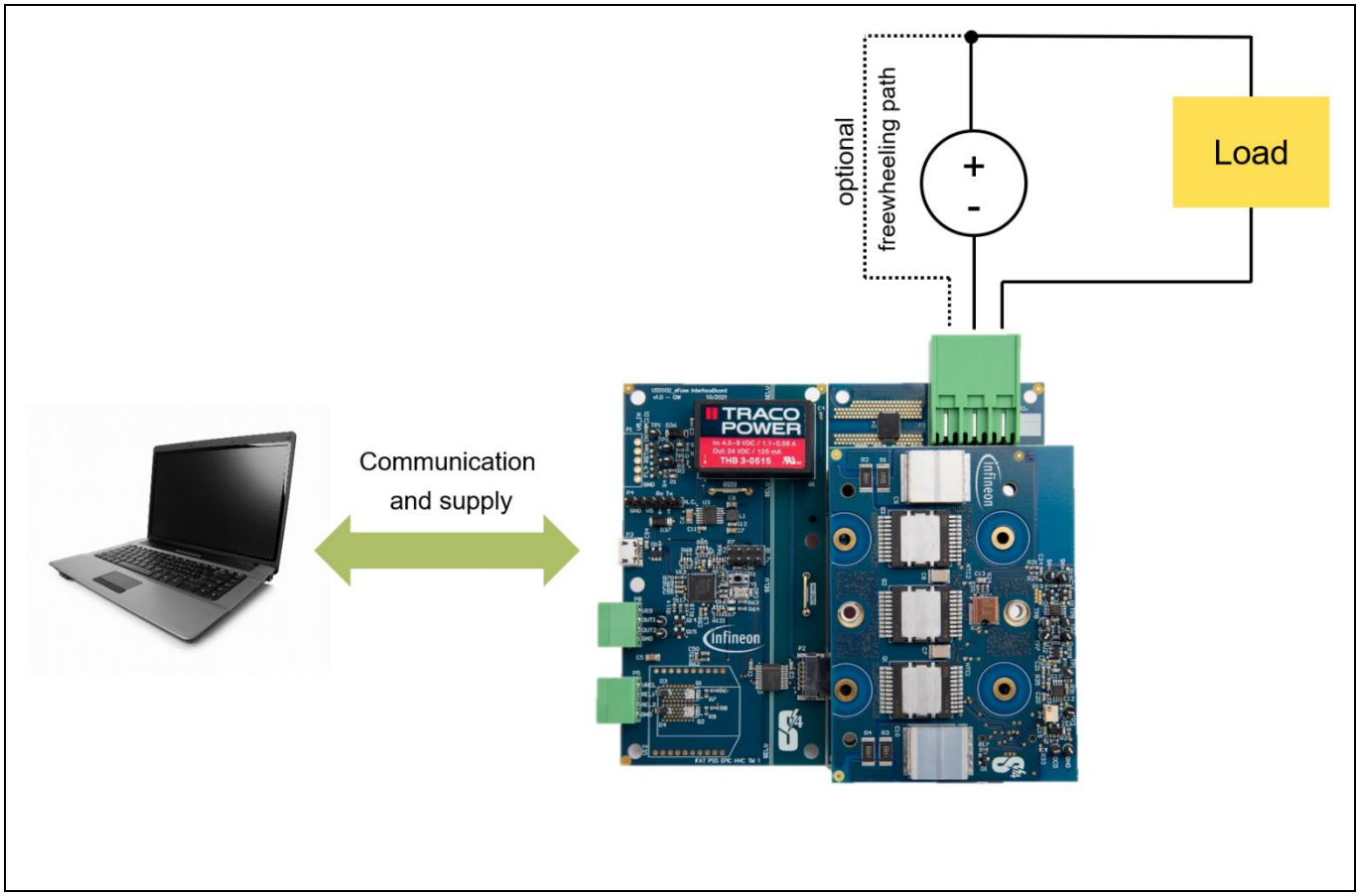

Figure 66 eFuse PoC basic startup setup

Attention: The eFuse PoC is designed as fuse application without any pre-charge circuitry. Turning on the eFuse if V_{DS} > 10 V is prohibited and is indicated by a fault flag!
Turn on the eFuse when the power supply voltage is below 10 V, or use external circuitry to pre-charge the load.

3.6 Communication Interface

The eFuse interface board acts as a gateway between the PC and the mainboard. The communication between the two boards is done via a galvanically isolated SPI and the mainboard is in slave configuration. The specifications for the SPI interface are shown in **Table 20** and **Figure 67**.

Table 20 SPI configuration of mainboard

Setting	Value
Word length	8 bits
Frame length	64 bits
Bus speed	2 MHz
Clock setting	MSB first Transmit on rising edge Receive on falling edge

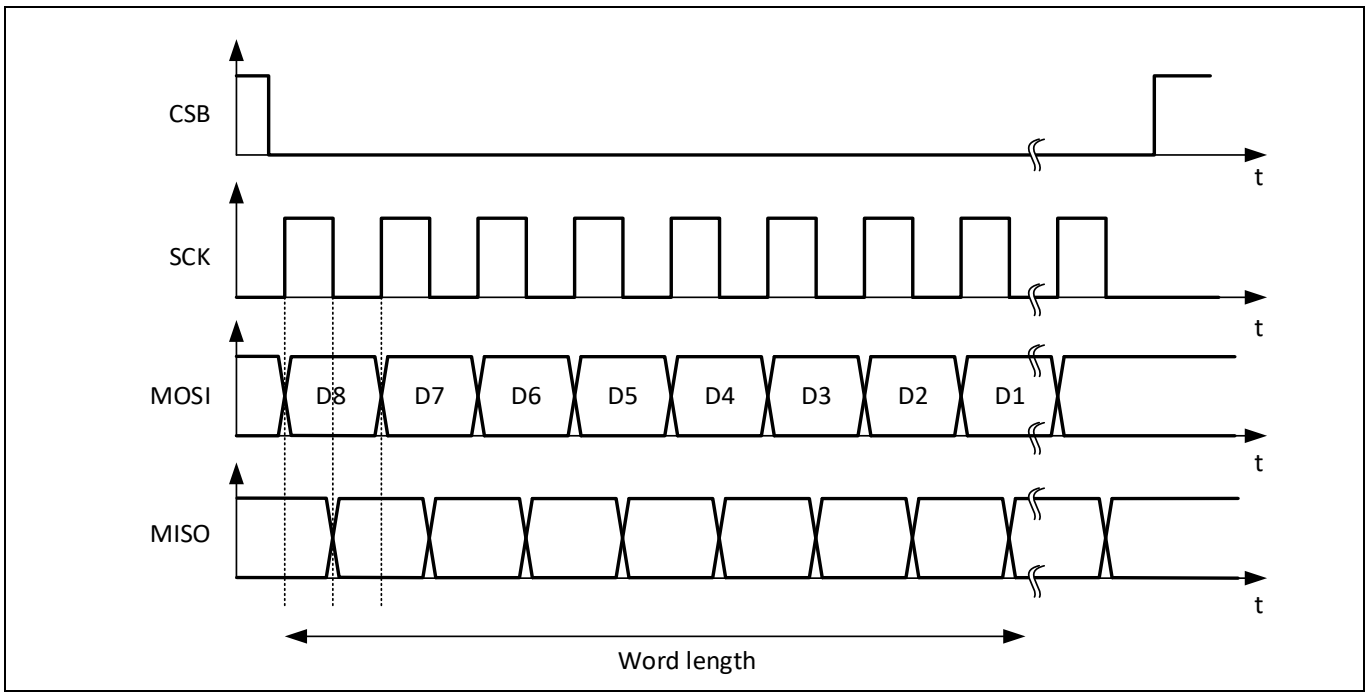

Figure 67 SPI frame structure for communication

3.6.1 SPI command list

Return data for each command will be returned with the following SPI command. Each SPI frame width is 8 bytes.

Table 21 SPI write data

Command	Byte number	Data	Description
EFUSE_ON	0	$0x23_h$	Turn eFuse switch on
	1	$0x24_h$	
EFUSE_ON	0	$0x23_h$	Turn eFuse switch off
	1	$0x25_h$	
EFUSE_RESET_ERROR	0	$0x23_h$	Reset all errors
	1	$0x26_h$	
EFUSE_TEST_OCD	0	$0x23_h$	Test OCD functionality
	1	$0x2D_h$	
EFUSE_TEST_DESAT	0	$0x23_h$	Test DESAT functionality
	1	$0x2C_h$	
EFUSE_SET_DESAT_THR	0	$0x23_h$	Set DESAT threshold
	1	$0x2E_h$	
	2	<var>	Threshold output PWM duty cycle high byte
	3	<var>	Threshold output PWM duty cycle low byte
EFUSE_SET_OCD_THR	0	$0x23_h$	Set OCD threshold
	1	$0x33_h$	
	2	<var>	Threshold output PWM duty cycle high byte
	3	<var>	Threshold output PWM duty cycle low byte
EFUSE_SET_SOH_THR	0	$0x23_h$	Set SOH diagnostic threshold
	1	$0x34_h$	
	2	<var>	Threshold output PWM duty cycle high byte
	3	<var>	Threshold output PWM duty cycle low byte
EFUSE_SHORT_PULSE	0	$0x23_h$	Turn eFuse on for a configurable short time (µs range)
	1	$0x29_h$	
	2	<var>	Pulse duration high byte
	3	<var>	Pulse duration low byte
EFUSE_OFF_CLEAR	0	$0x23_h$	Turn eFuse off and clear errors
	1	$0x36_h$	
EFUSE_GATE_LEAKAGE_TEST	0	$0x23_h$	Start gate leakage test sequence
	1	$0x38_h$	
EFUSE_SWITCH_SOH_TEST	0	$0x23_h$	Start SOH test sequence
	1	$0x39_h$	
EFUSE_CONFIG_OVERTEMP	0	$0x23_h$	Configure overtemperature warning and shutdown (in ADC value format)
	1	$0x3E_h$	

Command	Byte number	Data	Description
	2	<var>	OTW high byte
	3	<var>	OTW low byte
	4	<var>	OTS high byte
	5	<var>	OTS low byte
EFUSE_CONFIG_GDU_SUPPLY	0	$0x23_h$	Configure gate driver supply voltage
	1	$0x3F_h$	
	2	<var>	1…high voltage; 0…low voltage
EFUSE_SINGLE_PULSE	0	$0x23_h$	Turn on eFuse for single pulse (width in ms)
	1	$0x40_h$	
	2	<var>	Pulse length high byte
	3	<var>	Pulse length low byte
EFUSE_CONFIG_DESAT_COMP	0	$0x23_h$	Configure DESAT temperature compensation
	1	$0x42_h$	
	2	<var>	1…enable; 0…disable
EFUSE_READ_ADC_VAL	0	$0x31_h$	Readback analog values
	1	<var>	ADC val address (see Table 24)

Table 22 SPI return data

Command	Byte Number	Data	Description
EFUSE_STATUS (Standard feedback)	0	$0x23_h$	EFUSE_GATEWAY
	1	$0x35_h$	EFUSE_STATUS
	2	<var>	Status flags byte 0 (see Table 23)
	3	<var>	Status flags byte 1 (see Table 23)
EFUSE_READ_ADC_VAL	0	$0x31_h$	EFUSE_READ_ADC_VAL
	1	<var>	Status flags byte 0 (see Table 23)
	2	<var>	Status flags byte 1 (see Table 23)
	3	<var>	16bit analog value 1 lower byte
	4	<var>	16bit analog value 1 higher byte
	5	<var>	16bit analog value 2 lower byte
	6	<var>	16bit analog value 2 higher byte
EFUSE_GATE_LEAKAGE_TEST	0	$0x23_h$	EFUSE_GATEWAY
	1	$0x38_h$	EFUSE_GATE_LEAKAGE_TEST
	2	<var>	Status flags byte 0 (see Table 23)
	3	<var>	Status flags byte 1 (see Table 23)
	4	<var>	GateTest_Vdrop lower byte
	5	<var>	GateTest_Vdrop higher byte
	6	<var>	GateTest_Vdiff lower byte
	7	<var>	GateTest_Vdiff higher byte

Table 23 Status flags description

Bit number	Name	Description
0	SwitchState	MCU output / gate driver input level
1	OCDState	Shunt-based OCD
2	OCDLatchState	Any fault condition
3	DESATState	Latched overcurrent status (shunt or V_{DS}-based)
4	Fault	V_{DS}-based OCD status
5	I_OVC	Analog current measurement overload
6	OTW	Overtemperature warning (any temperature sensor)
7	OTS	Overtemperature shutdown (any temperature sensor)
8	VDRV_OV	Gate driver supply overvoltage
9	VDRV_UV	Gate driver supply undervoltage
10	VON_OV	Vfuse overvoltage error (Vfuse has to be <10 V for turn-on)

Table 24 Analog readback values address

Selected address	Name	Bytes	Description
0	AMEAS_V_CAP	*0:1*	Gate driver V_{DD} capacitor voltage
	AMEAS_V_DESAT_thr_read	*2:3*	DESAT threshold voltage
1	AMEAS_V_DRV	*0:1*	Gate driver supply voltage
	AMEAS_V_FUSE	*2:3*	Voltage measurement of fuse
2	AMEAS_V_GATE_RB	*0:1*	Gate voltage readback
	AMEAS_V_ISENSE	*2:3*	Shunt voltage measurement for current sense
3	AMEAS_V_NTC1	*0:1*	Discrete NTC1 voltage
	AMEAS_V_NTC2	*2:3*	Discrete NTC2 voltage
4	AMEAS_V_OCD_thr_read	*0:1*	OCD voltage threshold
	AMEAS_V_VDS_SENSE	*2:3*	V_{DS} voltage of fuse (in on state)
5	AMEAS_Vtemp1	*0:1*	On-die temperature sense diode stack voltage 1
	AMEAS_Vtemp2	*2:3*	On-die temperature sense diode stack voltage 2
6	AMEAS_Vtemp3	*0:1*	On-die temperature sense diode stack voltage 3
	<no data>	*2:3*	*Empty*
7	Time_SwitchON	*0:1*	Turn-on time of MOSFET
	Time_SwitchOFF	*2:3*	Turn-off time of MOSFET

All analog values are direct ADC values. Conversion factors for measurements are described in 0.

Table 25 Analog values conversion factors

ADC value	Conversion
General	$V_{ADC} = ADCval \cdot \frac{5}{4096}$
AMEAS_V_DRV, AMEAS_V_GATE_RB	$V_{ADC} = ADCval \cdot 0{,}009359$
AMEAS_V_FUSE	$V_{ADC} = ADCval \cdot \frac{5}{4096} \cdot 101$
AMEAS_V_NTC1, AMEAS_V_NTC2	Use NTC lookup table for calculations;
AMEAS_Vtemp1, AMEAS_Vtemp2, AMEAS_Vtemp3	$Temp_{die,x} = -146{,}82 + ADCval \cdot 411{,}16$
Time_SwitchON, Time_SwitchOFF	$t = ADCval \cdot 0{,}01041666$

Glossary

ADC	Analog-to-digital converter
BIST	Built in self-test
BMS	Battery main switch
BSC	Back side cooling
C_{th}	Thermal capacitance
DESAT	Desaturation
ECU	Electronic control unit
ESL	Equivalent series inductance
ESR	Equivalent series resistance
EV	Electric vehicle
FEM	Finite element method
GDU	Gate driver unit
GUI	Graphical user interface
HVAC	Heating, ventilation and air conditioning
IGBT	Insulated gate bipolar transistor
LSL	lower specification limit
MCU	Microcontroller
MOSFET	Metal oxide semiconductor field-effect transistor
MOV	Metal oxide varistor
NTC	Negative temperature coefficient
OCD	Overcurrent detection
OTS	Overtemperature shutdown
OTW	Overtemperature warning
PCB	Printed circuit board
PI	Polyimide
PoC	Proof of concept
PrePreg	Preimpregnated fibres
PTC heater	Positive temperature coefficient heating element
$R_{DS(on)}$	Resistance at the actual junction temperature, given at the datasheet current I_{DS}
R_{th}	Thermal resistance
SC	Short circuit
SELV	Safety extra low voltage
SMD	Surface mounted device
SOH	State of health
SPI	Serial peripheral interface
SPICE	Simulation program with integrated circuit emphasis
T_a	Ambient temperature
TIM	Thermal interface material
T_j	Junction temperature
TSC	Top-side cooling
TVS	Transient voltage suppressor
USB	Universal serial bus
USL	Upper specification limit
V_{DS}	Drain-source voltage
µC	Microcontroller
µVia	Microvia

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Revision history

Document version	Date	Description of changes
V 1.0	2022-12-22	Initial release

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Edition 2022-12-22

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
UM_2211_PL52_2212_165057

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